

8		7		6		5		4		3		2		1				
1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%. 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS. 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.												REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE	
												E		408158	PRODUCTION RELEASED	11/01/05	?	
												IMG5 17" REV E 11/01/05						
D	PDF	CSA	CONTENTS	SYNC	MASTER	DATE	PDF	CSA	CONTENTS	SYNC	MASTER	DATE	PDF	CSA	CONTENTS	SYNC	MASTER	DATE
	2	2	System Block Diagram	FINO-DD		06/20/2005	38	54	CPU AVDD VREG	FINO-HS		06/20/2005	74	132	Vesta Ethernet PHY	Q63		08/01/2005
	3	4	Power Block Diagram	FINO-PC		06/20/2005	39	55	T,V,I SENSORS	FINO-HS		06/20/2005	75	136	ETHERNET CONNECTOR	FINO-DC		06/20/2005
	4	5	Table Items	FINO-M23		08/26/2005	40	56	CPU ALIASES & MISC	FINO-HS		06/20/2005	76	138	Shasta FireWire	Q63		08/01/2005
	5	6	FUNC TEST 1 OF 2	FINO-ME		06/20/2005	41	58	KODIAC NBMEM PWR & CAPS	Q63		08/01/2005	77	139	Vesta FireWire PHY	Q63		08/01/2005
C	6	7	Power Conn / Alias	M23-PC		06/20/2005	42	59	Kodiak Memory Dq/Ctl	FINO-DS		06/20/2005	78	140	FIREWIRE CONNECTORS	FINO-DC		06/20/2005
	7	8	Signal Alias	FINO-DD		06/20/2005	43	61	Parallel Term	FINO-DS		06/20/2005	79	142	USB Host Interfaces	FINO-PC		07/05/2005
	8	9	FUNC TEST 2 OF 2	FINO-ME		06/20/2005	44	62	Main Memory Clock Buffer	FINO-DS		06/20/2005	80	143	USB Device Interfaces	FINO-PC		06/20/2005
	9	11	1.8V Vreg	M23-PC		06/20/2005	45	63	MEMORY ADDR BRANCHING	FINO-DS		06/20/2005	81	144	Flash Media Ctrl	FINO-PC		06/20/2005
	10	12	1.5V Vreg	FINO-PC		06/20/2005	46	67	Memory Dimm A	FINO-DS		06/20/2005	82	145	Flash Connector	FINO-PC		06/20/2005
	11	13	1.2V Vreg	FINO-PC		06/20/2005	47	68	MLB Mem Series Term	FINO-DS		06/20/2005	83	147	AUDIO: CODEC	FINO-SO		10/07/2005
	12	15	2.5V Vreg	FINO-PC		06/20/2005	48	69	On-Board DDR SDRAM	FINO-DS		06/20/2005	84	148	AUDIO: LINE INPUT AMP	FINO-SO		10/07/2005
	13	16	5V & 3.3V Fets	FINO-PC		06/20/2005	49	70	On-Board DDR SDRAM	FINO-DS		06/20/2005	85	150	AUDIO: LINE OUT AMP	FINO-SO		10/07/2005
	14	17	Vesta Core / Misc	FINO-DC		06/20/2005	50	82	KODIAK PCI-E X16	Q63		08/01/2005	86	152	AUDIO: SPEAKER AMP	FINO-SO		10/07/2005
	15	19	KODIAK CORE & BYPASS	Q63		08/01/2005	51	84	GPU PCIe	M23-DD		06/20/2005	87	153	AUDIO: CONNECTORS	FINO-SO		10/07/2005
B	16	20	KODIAK & SHASTA MISC	FINO-ME		06/20/2005	52	85	Graphics Vregs	M23-DD		06/20/2005	88	154	AUDIO: POWER SUPPLIES	FINO-SO		10/07/2005
	17	23	Shasta Core Power	Q63		08/01/2005	53	86	GPU Core Power	FINO-DD		06/20/2005						
	18	24	Shasta Serial / Misc	FINO-ME		06/20/2005	54	87	GPU Frame Buffer	FINO-DD		06/20/2005						
	19	25	PULSAR2 POWER	Q63		08/01/2005	55	88	FB Series Termination	FINO-DD		06/20/2005						
	20	26	PULSAR2 CLOCKS	FINO-ME		06/20/2005	56	89	GPU GDDR SDRAM A	FINO-DD		06/20/2005						
	21	27	Pulsar Aliases	FINO-ME		06/20/2005	57	90	GPU GDDR SDRAM B	FINO-DD		06/20/2005						
	22	28	System Management Unit	Q63		08/01/2005	58	92	GPU Straps	FINO-DD		06/20/2005						
	23	29	SMU SUPPLEMENTAL (2)	FINO-HS		06/20/2005	59	93	GPU DVI & DACs	FINO-DD		06/20/2005						
	24	30	SMU SUPPLEMENTAL (3)	FINO-HS		06/20/2005	60	96	TMDS/Inverter/ExtVGA	M23-DD		06/20/2005						
	25	31	SMU SUPPLEMENTAL (4)	FINO-HS		06/20/2005	61	97	KODIAK PCI-E CONST	FINO-DD		06/20/2005						
A	26	32	Fan 0, 1 & System Temp	FINO-HS		06/20/2005	62	98	KODIAK HT16	Q63		08/01/2005						
	27	33	Fan 2 & HD Temp	FINO-HS		06/20/2005	63	101	HT ALIASES	FINO-ME		06/20/2005						
	28	39	I2C Connections	FINO-ME		06/20/2005	64	103	Shasta HyperTransport	Q63		08/01/2005						
	29	41	KODIAK EI PWR & CAPS	Q63		08/01/2005	65	119	Shasta PCI Interface	Q63		08/01/2005						
	30	42	KODIAK EI A	Q63		08/01/2005	66	120	PCI SERIES TERMINATION	FINO-MW		06/20/2005						
	31	43	CPU EI AND IO	FINO-HS		06/20/2005	67	121	AIRPORT & BLUETOOTH	FINO-MW		06/20/2005						
	32	44	KODIAK EI B	Q63		08/01/2005	68	122	USB 2.0 PCI Interface	Q63		08/01/2005						
	33	47	CPU STRAPS	FINO-HS		06/20/2005	69	125	BootROM	Q63		08/01/2005						
	34	48	CPU POWER AND BYPASS	FINO-HS		06/20/2005	70	127	Shasta Disk	M23-DC		06/20/2005						
	35	49	PROC DECOUPLING	FINO-HS		06/20/2005	71	129	Disk Connectors	M23-DC		06/20/2005						
A	36	50	CPU VCORE VREG	M23-HS		06/20/2005	72	130	ENET SERIES TERM	FINO-DC		06/20/2005						
	37	52	CPU VCORE MORE BYPASS	FINO-HS		06/20/2005	73	131	Shasta Ethernet	Q63		08/01/2005						
8		7		6		5		4		3		2		1				

DIMENSIONS ARE IN MILLIMETERS


XX : \_\_\_\_\_

X.XX : \_\_\_\_\_

X.XXX : \_\_\_\_\_

ANGLES : \_\_\_\_\_

DO NOT SCALE DRAWING



THIRD ANGLE PROJECTION

METRIC

DRAFTER

ENG APPD

QA APPD

RELEASE

DESIGN CK

MFG APPD

DESIGNER

SCALE

SIZE

D

MATERIAL/FINISH

NOTED AS

APPLICABLE

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TITLE

SCH,MLB,IMG5,17

DRAWING NUMBER

051-6790

REV.

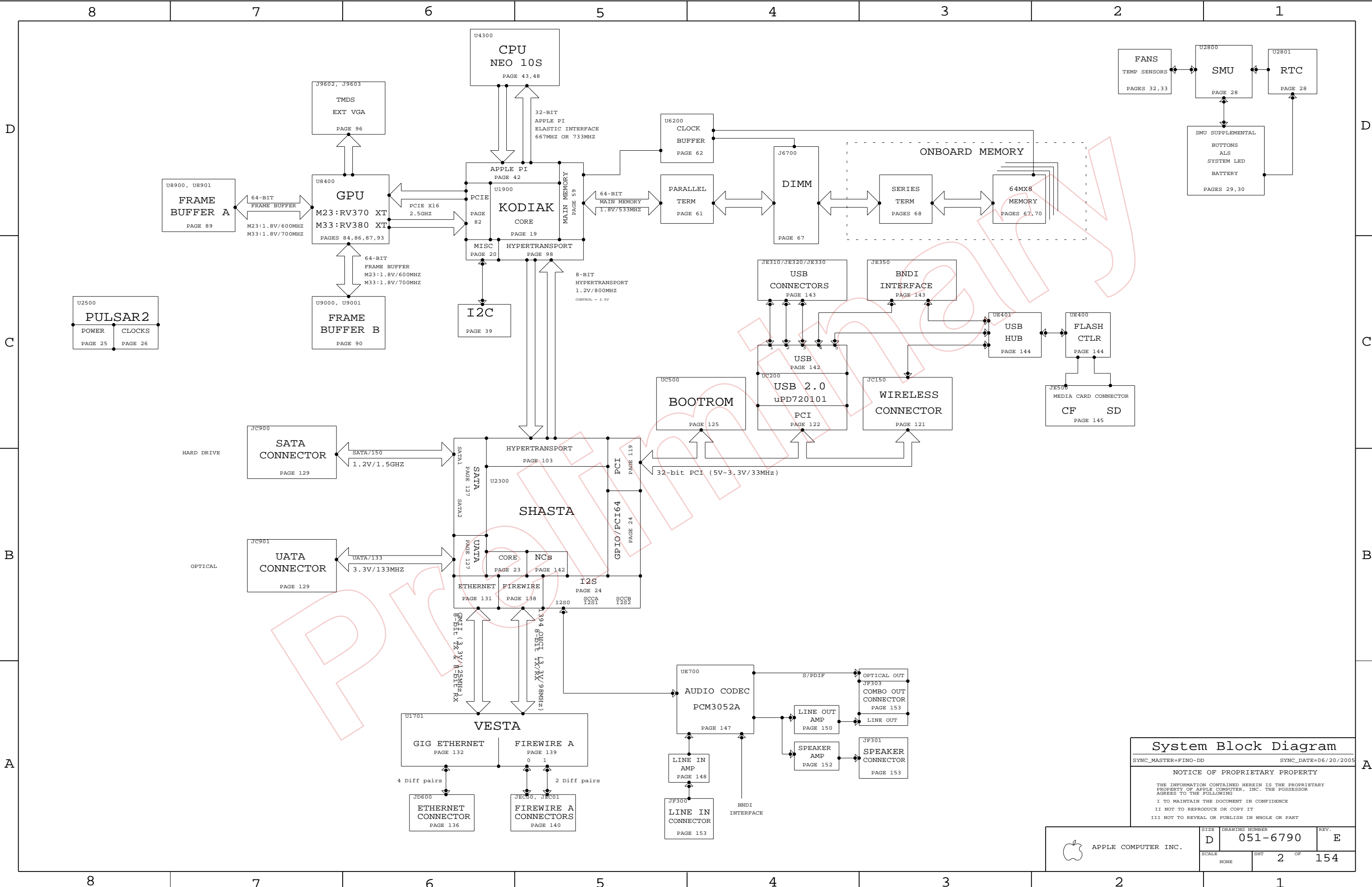
E

SHT

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OF

154



**System Block Diagram**

SYNC\_MASTER=FINO-DD SYNC\_DATE=06/20/2005

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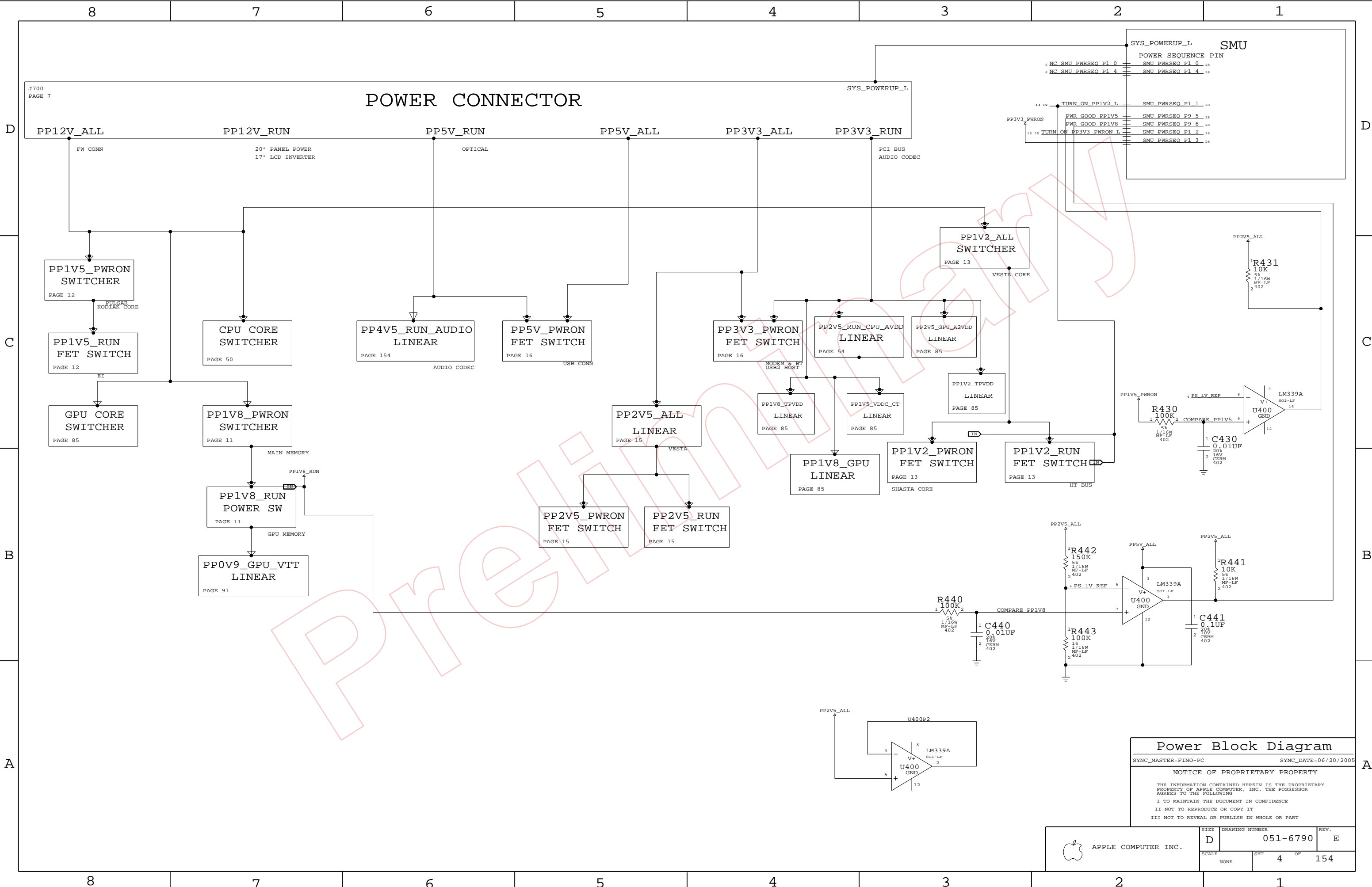
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SCALE	NONE	SHT	2 OF 154



Power Block Diagram

SYNC\_MASTER=FINO-PC

SYNC\_DATE=06/20/2005

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	D	051-6790	E
SCALE		SHT	OF
NONE		4	154

8		7		6		5		4		3		2		1		
PROCESSORS												ASICS				
NEED TO UPDATED BIN CODES AS NOTES																
PART #		QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION					
337S3224		1	PROCESSOR	CBGA-576-1MM	IC,GPUL,DD3.1,1.9G,85C	1.9GHZ	1.10V	45W	50MV	U4300	17_INCH_LCD	CRITICAL				
337S3220		1	PROCESSOR	CBGA-576-1MM	IC,GPUL,DD3.1,2.1G,85C	2.1GHZ	1.10V	45W	50MV	U4300	20_INCH_LCD	CRITICAL				
PART NUMBER		ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:											
337S3225		337S3224	17_INCH_LCD	U4300	IC,DD3.1,1.9G,1.15V											
337S3226		337S3224	17_INCH_LCD	U4300	IC,DD3.1,1.9G,1.20V											
337S3227		337S3224	17_INCH_LCD	U4300	IC,DD3.1,1.9G,1.25V											
337S3228		337S3224	17_INCH_LCD	U4300	IC,DD3.0X,1.9G,1.15V											
337S3229		337S3224	17_INCH_LCD	U4300	IC,DD3.0X,1.9G,1.20V											
337S3230		337S3224	17_INCH_LCD	U4300	IC,DD3.0X,1.9G,1.25V											
337S3231		337S3224	17_INCH_LCD	U4300	IC,DD3.0X,1.9G,1.30V											
337S3221		337S3220	20_INCH_LCD	U4300	IC,DD3.1,2.1G,1.15V											
337S3222		337S3220	20_INCH_LCD	U4300	IC,DD3.1,2.1G,1.20V											
337S3223		337S3220	20_INCH_LCD	U4300	IC,DD3.1,2.1G,1.25V											
												MISC PARTS				
PART#		QTY	DESCRIPTION		REFERENCE DESIGNATOR(S)		BOM OPTION									
051-6790		1	PCB,SCHEM,MLB,M23		SCH1		17_INCH_LCD									
051-6863		1	PCB,SCHEM,MLB,M33		SCH1		20_INCH_LCD									
820-1783		1	PCB,FAB,MLB,M23		MLB1		17_INCH_LCD		CRITICAL							
820-1766		1	PCB,FAB,MLB,M33		MLB1		20_INCH_LCD		CRITICAL							
062-2082		1	SPEC,VENDOR PACKAGING PROCEDURE		VPP1											
825-6447		1	BARCODE LABEL, MLB		LBL1											
341T1751		1	IC,FLASH,1MX8,3.3V,90NS		UC500				CRITICAL							
341T1752		1	PURCH ASSY, SMU BIG		U2800				CRITICAL							
603-7318		1	M23 CPU HEATSINK		MECH1		OMIT		CRITICAL							
603-7321		1	M33 CPU HEATSINK		MECH1		OMIT		CRITICAL							
603-7319		1	M23 GPU HEATSINK		MECH2		OMIT		CRITICAL HEATSINKS ARE NOW ON THE PD BOM							
603-7322		1	M33 GPU HEATSINK		MECH2		OMIT		CRITICAL							
603-7320		1	M23 NB HEATSINK		MECH3		OMIT		CRITICAL							
603-7323		1	M33 NB HEATSINK		MECH3		OMIT		CRITICAL							
875-1905		1	CPU GAP FILLER		GAP1											
875-2429		1	LED COVER TAPE		TAPE1		17_INCH_LCD									
												ALTERNATES				
PART NUMBER		ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:											
378S0140		378S0141		LED700,LED702	KINGBRIGHT LED											
343S0388		343S0356		U1701	VESTA A4											
126S0078		126S0086		C722	EL CAP											
126S0068		126S0088		CF000	EL CAP											
353S1321		353S1105		U400	LM339											
138S0558		138S0547			10UF CAP ALL LOC.											
124-0338		124-0333			PANASONIC CAPS											
Table Items																
SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005																
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												D	051-6790		E	
												SCALE	SHT	OF		
												NONE	5	154		



NO TEST XW NETS

NO TEST=

YES

GND U1100 11

124

NO TEST=

YES

GND U1200 12

125

NO TEST=

YES

GND U1300 13

126

NO TEST=

YES

PP 2V5PWRONNBMISC 20

127

NO TEST=

YES

PP 1V2PWRONSBVCORE 23

128

NO TEST=

YES

PP 3V3PWRONSBPC164 23

129

NO TEST=

YES

PP 2V5PWRONSB 23

130

NO TEST=

YES

PP 1V2PWRONSBELL45VDD 24

131

NO TEST=

YES

PP OVDD PULSAR1 25

132

NO TEST=

YES

PP 1V2PWRONPULSAR1 25

133

NO TEST=

YES

PP 1V5PULSAR2 25

134

NO TEST=

YES

PP 1V5PWRONPULSAR2 25

135

NO TEST=

YES

GND SMU AVSS 28 55

136

NO TEST=

YES

PP 3V3ALLSMUAVCC 28

137

NO TEST=

YES

PP 3V3ALLSMU 28

138

NO TEST=

YES

PP VE1NB 41

139

NO TEST=

YES

GND CPU AVDD 48

140

NO TEST=

YES

VC AGND 50

141

NO TEST=

YES

VC OUTSEN R 50

142

NO TEST=

YES

KPVD02 FMAX 55

143

NO TEST=

YES

GND GPU PVSS 86

144

NO TEST=

YES

GND GPU MPVSS 87

145

NO TEST=

YES

GND AUDIO MIC 153 154

146

NO TEST=

YES

GND GPU TPVSS 93

147

NO TEST=

YES

GND GPU TVXSSR 93

148

NO TEST=

YES

GND GPU VSSD1 93

149

NO TEST=

YES

GND GPU AVSSN 93

150

NO TEST=

YES

GND GPU AVSSQ 93

151

NO TEST=

YES

GND GPU A2VSSN 93

152

NO TEST=

YES

GND GPU A2VSSQ 93

153

NO TEST=

YES

KOD L15 GND 98 101

154

NO TEST=

YES

PP 3V3SBPCI B9 99

155

NO TEST=

YES

PP 2V5PWRONSB B9 119

156

NO TEST=

YES

PP VIOPCIUSB2 C2 122

157

NO TEST=

YES

PP 1V2PWRONDISKSB CC 127

158

NO TEST=

YES

PP2V5\_VESTA\_BIASVDD1 132

159

NO TEST=

YES

PP2V5\_VESTA\_XTALVDD1 132

160

NO TEST=

YES

PP1V2\_VESTA\_PLLVDD1 132

161

NO TEST=

YES

PP1V2\_VESTA\_PLLVDD2 139

162

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PP2V5\_VESTA\_BIASVDD2 139

163

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PP2V5\_VESTA\_XTALVDD2 139

164

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PP1V2\_VESTA\_FAVDDL 139

165

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YES

PP2V5\_VESTA\_FAVDDM 139

166

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YES

PP3V3\_VESTA\_FAVDDH 139

167

NO TEST=

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PP3V3\_PWRON\_NEC\_AVDD 142

168

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YES

GND AUD LOAMP 150 154

169

NO TEST=

YES

GND NEC AVSS R 142

170

NO TEST=

YES

GND AUDIO SPKRAMP PLANE 152 154

171

NO TEST=

YES

GND AUDIO CODEC 147 148 150 154

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KPGND2\_FMAX 55

173

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TDIODE\_POS\_FMAX 55

174

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TDIODE\_NEG\_FMAX 55

175

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DAGND 55

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INA138\_OUT 55

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NO TEST=

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RAMCLK\_AVSS 62

178

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PP12V\_AUDIO\_SPKRAMP 7152

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GND AUDIO 7154

180

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YES

GND AUDIO SPKRAMP 7152 154

181

NO TEST=

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KOD\_H05\_GND 82 97

182

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KOD\_K07\_GND 82 97

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KOD\_G10\_GND 82 97

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KOD\_J13\_GND 82 97

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KOD\_L13\_GND 82 97

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KOD\_H08\_GND 82 97

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PCIE\_SLOT\_PRESNT\_L 82 84

188

NO TEST=

YES

U8500\_GND 85

189

NO TEST=

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GND AUD LOAMP\_CHGMP 150 154

190

NO TEST=

YES

TP FBBCS1\_L 87

191

NO TEST=

YES

AUD\_4V5\_FB 154

192

NO TEST=

YES

ITS\_RUNNING 7

193

NO TEST=

YES

LED801\_1 8

194

NO TEST=

YES

LED802\_1 8

195

NO TEST=

YES

PCI\_CLK66M\_SB\_INT\_R 26

196

NO TEST=

YES

Q800\_D 8

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NO TEST=

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Q800\_G 8

198

NO TEST=

YES

Q801\_B 8

199

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Q802\_B 8

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Q802\_E 8

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Q803\_B 8

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TP\_SB\_PLITEST 24

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TP USB2\_PWREN<3> 143

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TP USB2\_PWREN<4> 143

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TP\_NEC\_NTEST1 122

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YES

TP\_NEC\_SMC 122

211

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YES

TP\_NEC\_SMI\_L 102

212

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YES

TP\_NEC\_SRCLK 122

213

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YES

TP\_NEC\_SRM0D 122

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YES

TP\_NEC\_TEST 122

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UATA\_DASP\_L\_DS 129

216

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RAM\_DQ\_R<60> 61 68 70

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RAM\_DQ\_R<59> 61 68 70

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RAM\_DQ\_R<30> 61 68 69

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RAM\_DQ\_R<21> 61 68 69

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NO TEST=

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RAM\_DQ\_R<14> 61 68 69

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RAM\_DQ\_R<13> 61 68 69

268

NO TEST=

YES

RAM\_DQ\_R<12> 61 68 69

269

NO TEST=

YES

RAM\_DQ\_R<11> 61 68 69

270

EE IDENTIFIED NO TEST NETS

NO TEST=

YES

NC\_EI\_NB\_TO\_CPU\_B\_CLK\_P 56

271

NO TEST=

YES

NC\_EI\_NB\_TO\_CPU\_B\_CLK\_N 56

272

NO TEST=

YES

NC\_EI\_NB\_TO\_CPU\_B\_AD<0..43> 56

273

NO TEST=

YES

NC\_EI\_NB\_TO\_CPU\_B\_SR\_P<0..1> 56

274

NO TEST=

YES

NC\_EI\_NB\_TO\_CPU\_B\_SR\_N<0..1> 56

275

NO TEST=

YES

NC\_EI\_CPU\_B\_TO\_NB\_CLK\_P 56

276

NO TEST=

YES

NC\_EI\_CPU\_B\_TO\_NB\_CLK\_N 56

277

NO TEST=

YES

NC\_EI\_CPU\_B\_TO\_NB\_AD<0..43> 56

278

NO TEST=

YES

NC\_EI\_CPU\_B\_TO\_NB\_SR\_P<0..1> 56

279

NO TEST=

YES

NC\_EI\_CPU\_B\_TO\_NB\_SR\_N<0..1> 56

280

NO TEST=

YES

NC\_NB\_CPU\_A1\_INT\_L 56

281

NO TEST=

YES

NC\_NB\_CPU\_B0\_INT\_L 56

282

NO TEST=

YES

NC\_NB\_CPU\_B1\_INT\_L 56

283

NO

D

C

B

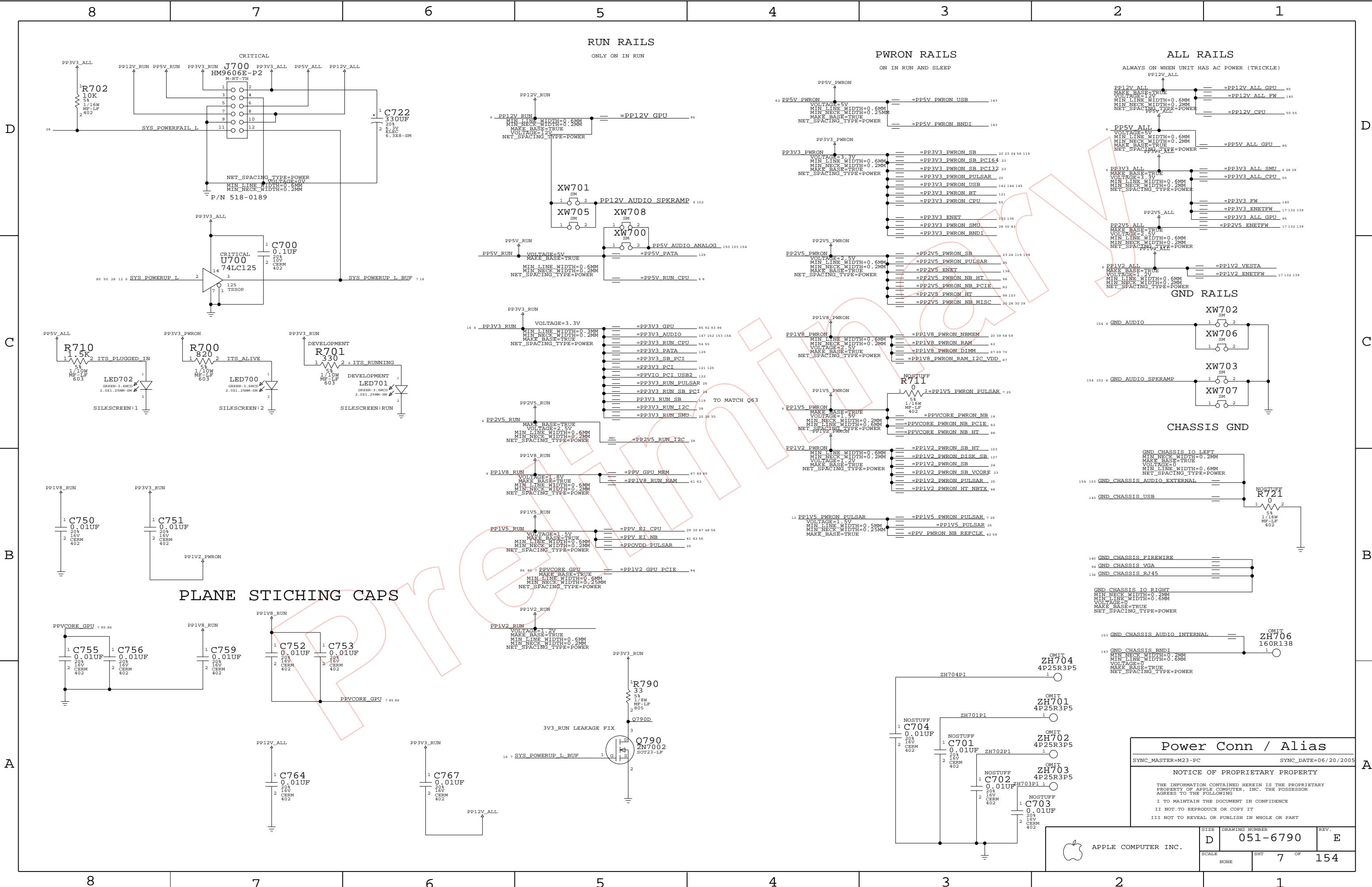
A

D

C

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A



Power Conn / Alias

SYNC\_MASTER=M23-PC

SYNC\_DATE=06/20/2005

NOTICE OF PROPRIETARY PROPERTY

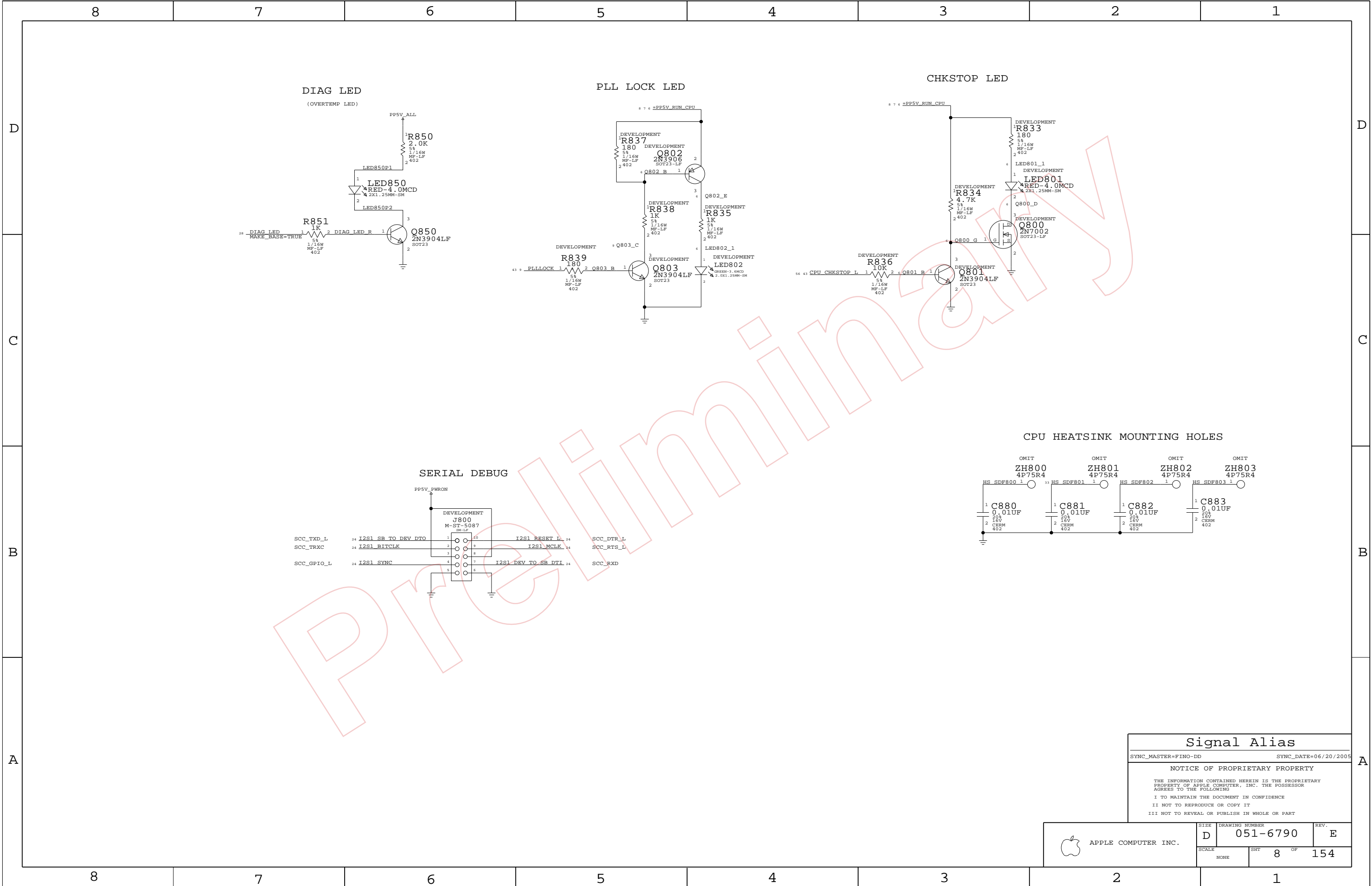
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	E
SCALE		SHT	7 OF 154
NONE			









## D

B

D

C

B

 $\lambda$ 

SIZE	DRAWING NUMBER	REV.
D	051-6790	E

SCALE	SHT	11	OF	154
NONE				

# KODIAK CORE VOLTAGE REGULATOR

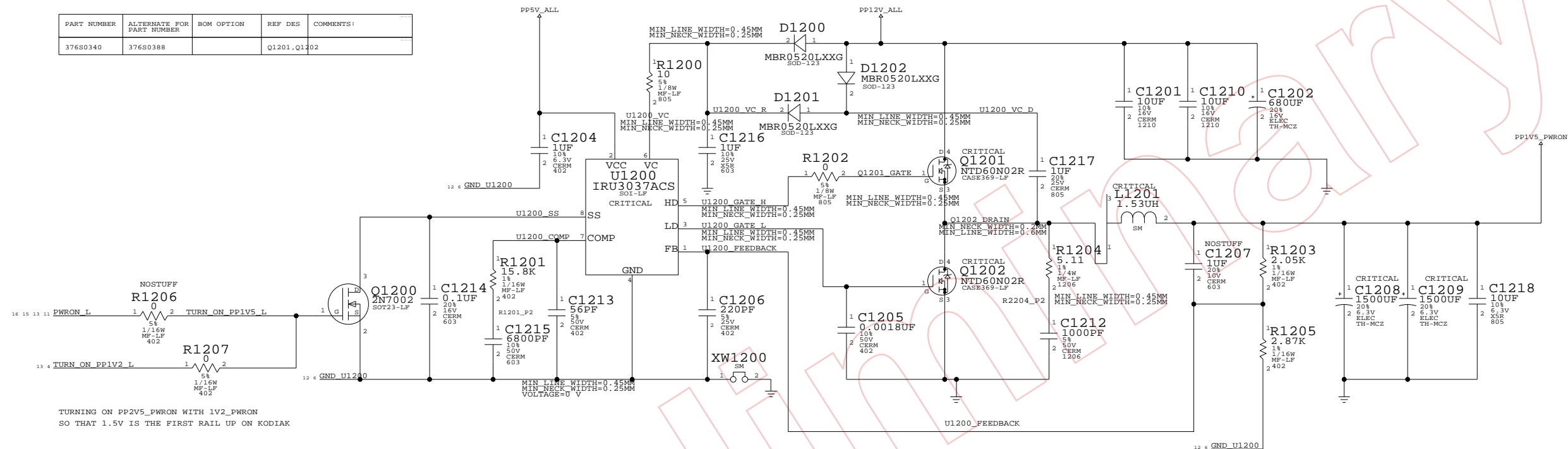
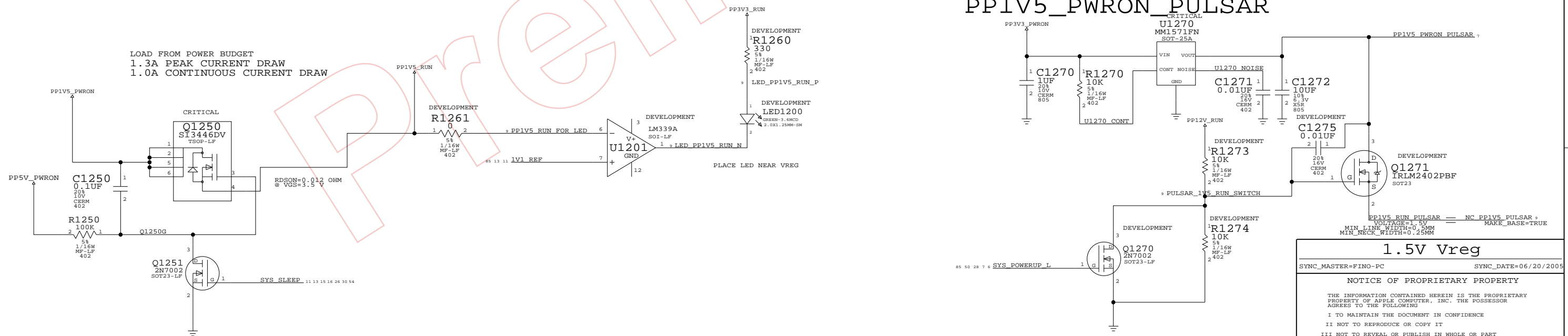
NOTE :

IRU3037ACS VREF=0.8VDC  
 $V_{OUT}=V_{REF} \cdot (R_{1203}+R_{1205})/R_{1205}=1.25VDC$

LOAD FROM POWER BUDGET  
8.5A PEAK CURRENT DRAW  
7.2A CONTINUOUS CURRENT DRAW

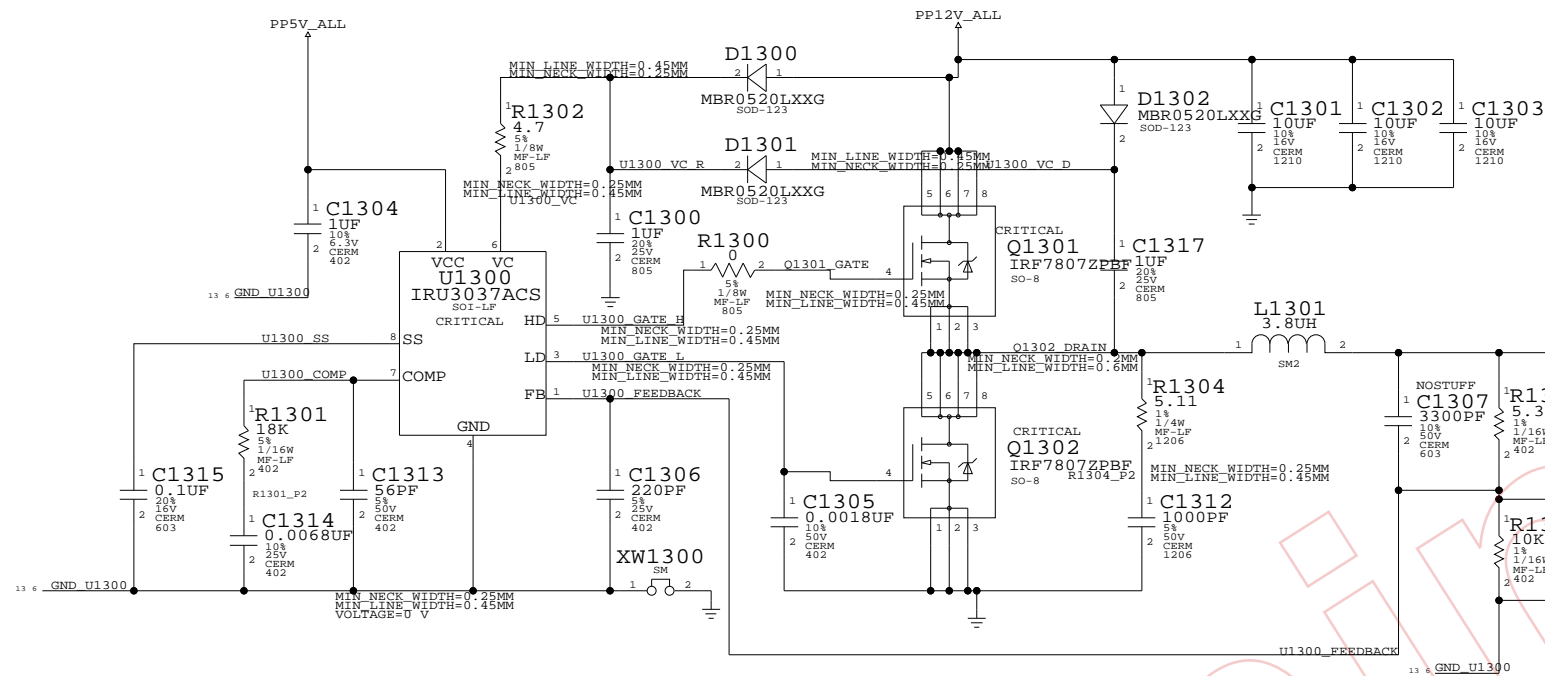
1.35V	R1205=2.87K
1.30V	R1205=3.24K
1.25V	R1205=3.65K

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0340	376S0388		Q1201,Q1202	

PP1V5 PWRON PULSAR

1.5V Vreg	
SYNC_MASTER=FINO-PC	SYNC_DATE=06/20/2005
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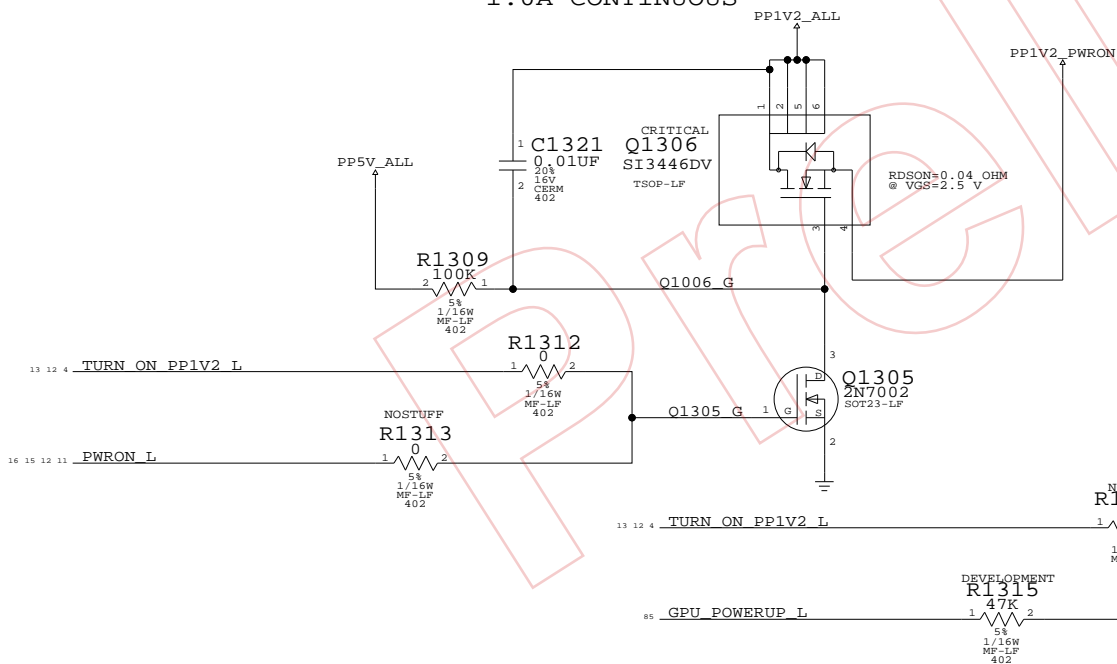
PP1V2\_ALL VOLTAGE REGULATOR



NOTE:  
SET OUTPUT=1.22-1.23V  
IRU3037ACS VREF=0.8VDC  
VOUT=VREF\*(R1003+R1005)/R1005=1.22-1.23VDC  
  
POWER BUDGET CURRENT OF TOTAL RAILS  
3.2A PEAK  
2.6A CONTINUOUS

PP1V2\_PWRON FET SWITCH

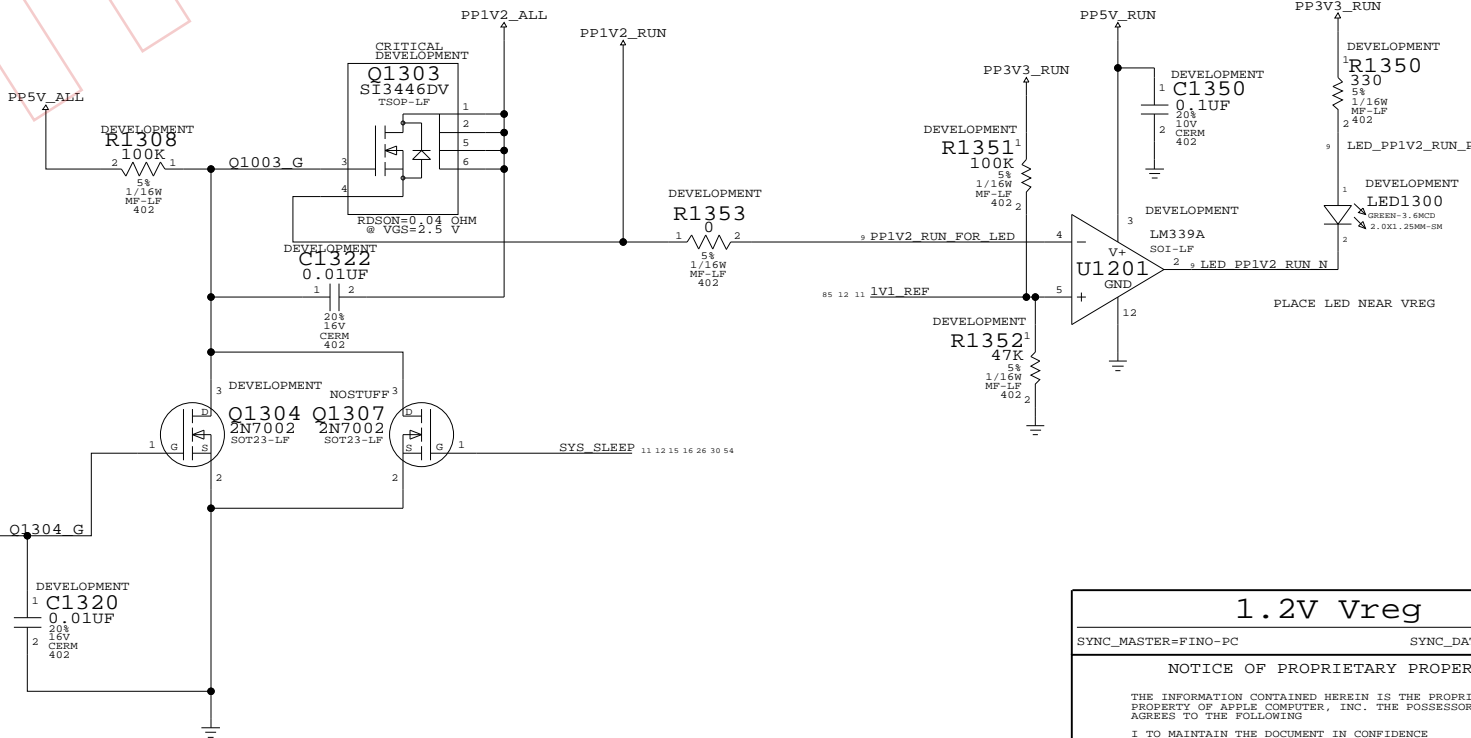
PEAK CURRENT 1.3A  
1.0A CONTINUOUS



PP1V2\_PWRON COMES UP BEFORE GPU\_POWERUP\_L SO THAT SHASTA CORE GETS POWER BEFORE ANYTHING ELSE

PP1V2\_RUN FET SWITCH

PEAK CURRENT 1.3A IF KODIAK 1.2V CAN BE TURNED OFF IN SLEEP. 0.6A/M33 0.0A/M23 IF NOT



1.2V Vreg

SYNC\_MASTER=FINO-PC SYNC\_DATE=06/20/2005

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SIZE D DRAWING NUMBER 051-6790 REV. E

SCALE NONE SHT 13 OF 154

## D




D

C

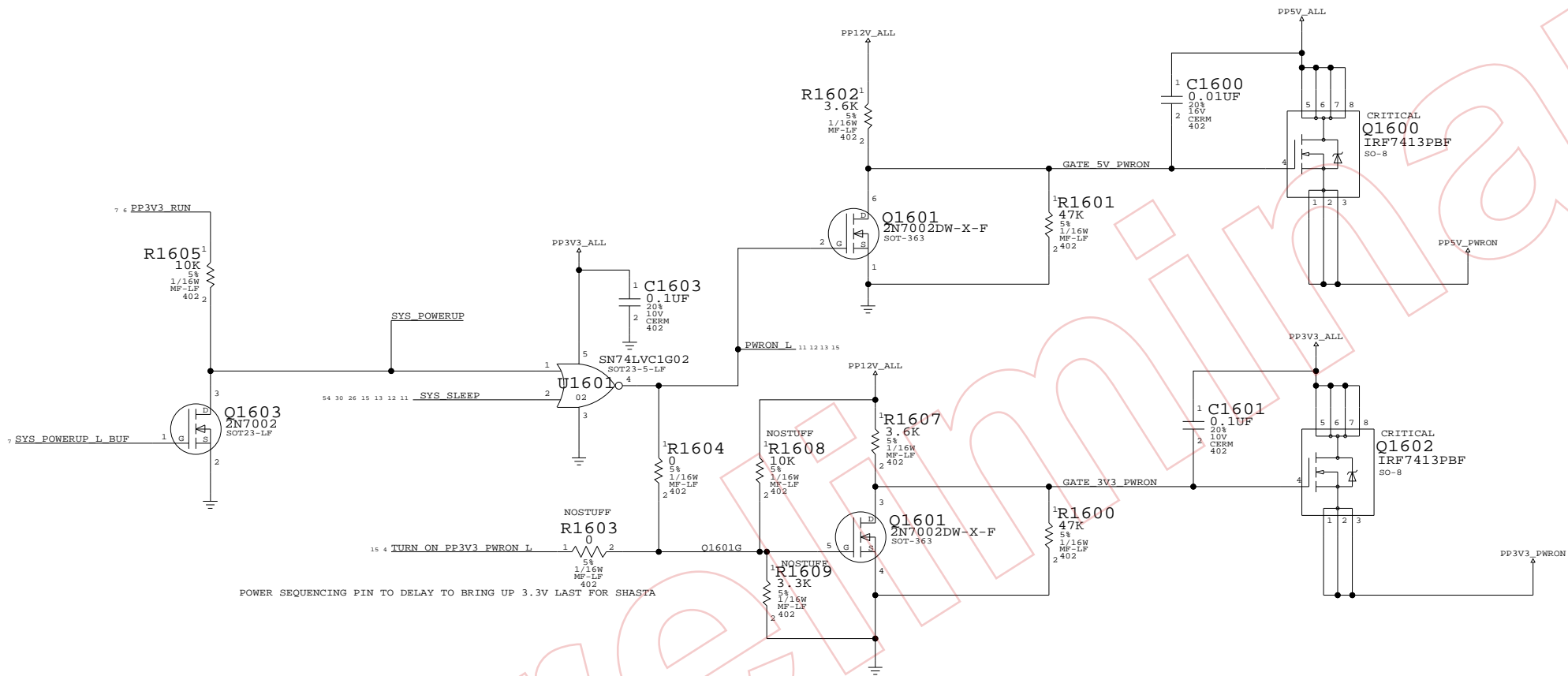
## B

B

A

 APPLE COMPUTER INC.8





## 5V & 3.3V Fets

SYNC\_MASTER=FINO-PC SYNC\_DATE=06/20/2005

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE	SHT	16 OF 154
NONE		

## Page Notes

Power aliases required by this page:

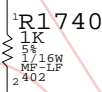
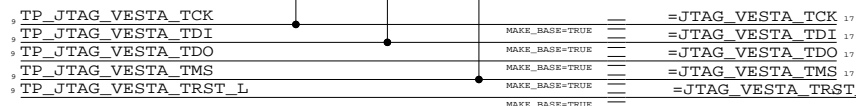
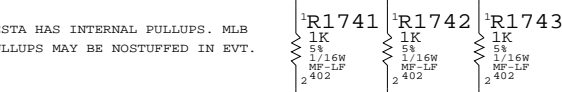
Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
- VESTA1V2\_BURST / VESTA1V2\_PULSE  
Controls operating mode of Vesta 1.2V regulator. If both options are off the regulator will be in continuous mode.

### VESTA JTAG

139 132 17 7 =PP3V3\_ENETFW

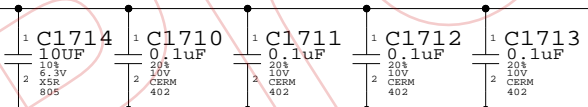
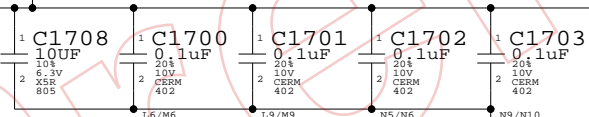
VESTA HAS INTERNAL PULLUPS. MLB  
PULLUPS MAY BE NOSTUFFED IN EVT.



M23: ADDED C1726 AND C1744 PER BROADCOM RECOMMENDATIONS

139 132 7 =PP1V2\_ENETFW

L1700 FERR-EMI-600-OHM  
MIN\_LINK\_WIDTH=0.50 MM  
MIN\_NECK\_WIDTH=0.25 MM  
VOLTAGE=1.2V



139 132 17 7 =PP3V3\_ENETFW

R1752 10K  
5%  
1/16W  
MF-LP  
402

RESET ASSERT REQUIREMENT\* IS 20MS TO 100MS

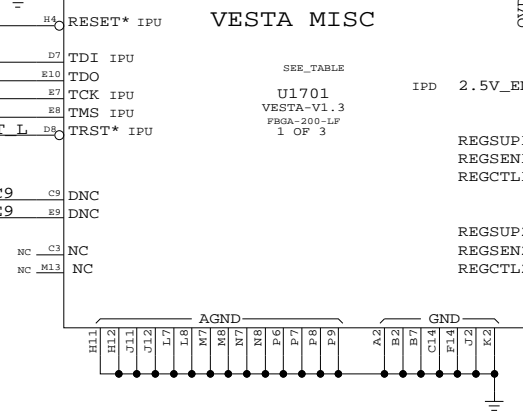
Q1750 2N7002DW-X-F  
SOT-363

132 VESTA RESET H

To keep Vesta from being held  
in reset when system is off  
NOTE: Reset GPIO is active HIGH

### VESTA MISC

U1701 VESTA-V1.3  
FPGA-200-LP  
1 OF 3



TP VESTA 2.5V\_EN

REGSUP1 TP VESTA REGSUP1  
REGSEN1 TP VESTA REGSEN1  
REGCTL1 TP VESTA REGCTL1

REGSUP2 TP VESTA REGSUP2  
REGSEN2 TP VESTA REGSEN2  
REGCTL2 TP VESTA REGCTL2

AGND

GND

### Vesta Core / Misc

SYNC\_MASTER=FINO-DC SYNC\_DATE=06/20/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE	SHT	OF
NONE	17	154



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C

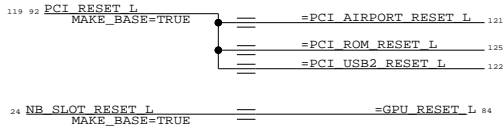
B

A

87654321

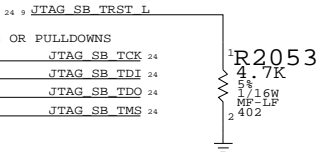
SHASTA ALIASES

PCI\_RESET\_L IS AN 'AND' OF SB\_PCI\_RESET\_L (SB)  
AND SYS\_IO\_RESET\_L (SMU)

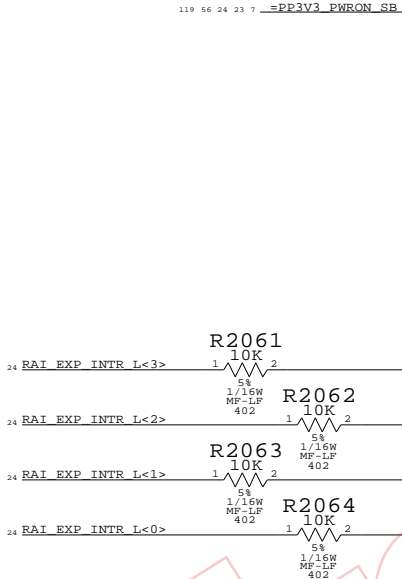


SHASTA JTAG

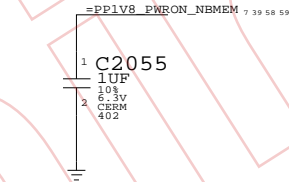
THESE PINS HAVE INTERNAL PULLUPS OR PULLDOWNS  
TP JTAG SB\_TCK  
MAKE\_BASE=TRUE  
=JTAG SB\_TCK 24  
TP JTAG SB\_TDI  
MAKE\_BASE=TRUE  
=JTAG SB\_TDI 24  
TP JTAG SB\_TDO  
MAKE\_BASE=TRUE  
=JTAG SB\_TDO 24  
TP JTAG SB\_TMS  
MAKE\_BASE=TRUE  
=JTAG SB\_TMS 24



SHASTA GPIO TERMINATIONS  
(SOME OF THESE ARE NOSTUFF  
ON PAGE 24 )

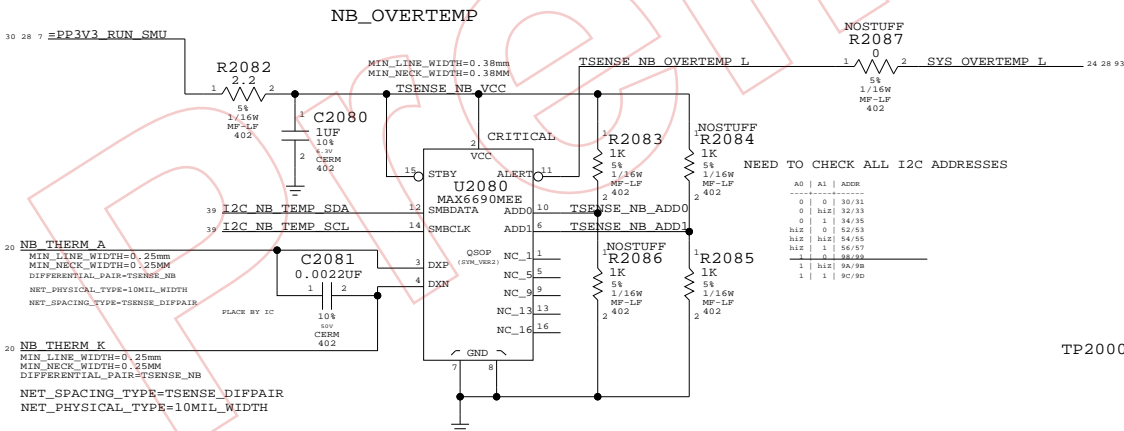
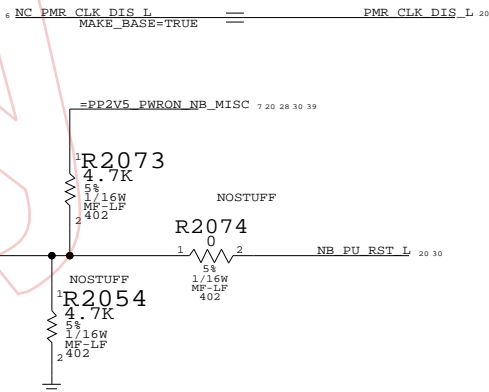


KODIAK JTAG\_TRST PULLED HIGH  
TO ALLOW SMU DEBUG ACCESS

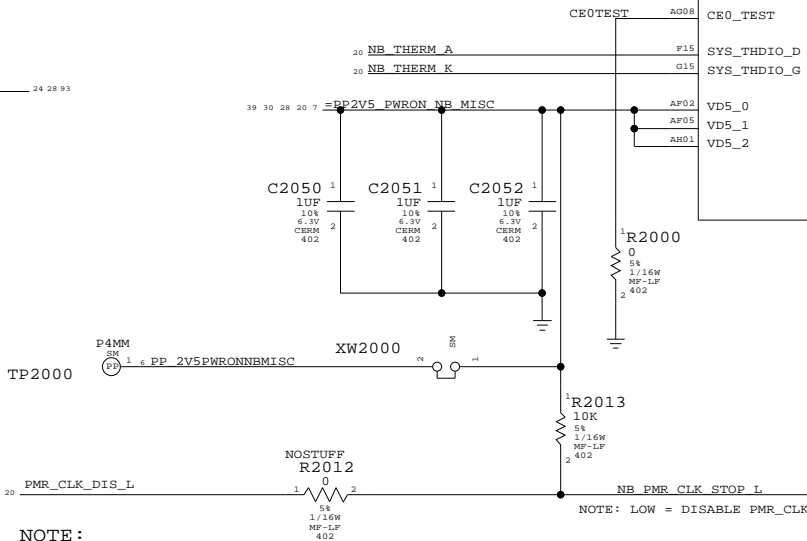


C2055 ADDED FOR KODIAK RAM DECOUPLING  
PAGE 58 IS SHORT ONE CAP

KODIAK ALIASES

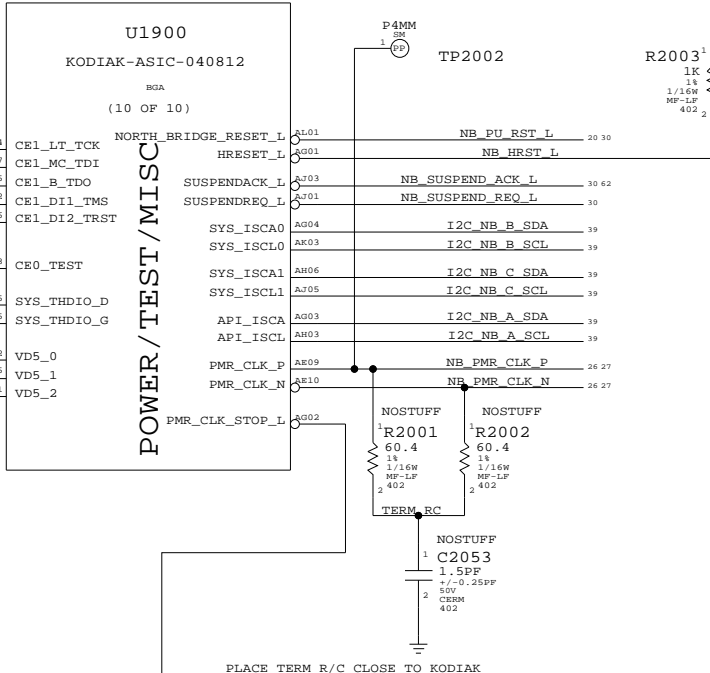


NEED TO CHECK ALL I2C ADDRESSES  
AD | AI | ADDR  
0 | 0 | 30/31  
0 | hi| 32/33  
0 | 1 | 34/35  
hi| 0 | 36/37  
hi| hi| 38/39  
1 | hi| 40/41  
1 | 1 | 42/43



NOTE:  
PMR\_CLK\_STOP CAN BE USED TO STOP ALL CLOCKS IN KODIAK  
USED FOR DEBUG  
PLACE R2012 IN AN ACCESSIBLE LOCATION

POWER/TEST/MISC



KODIAK & SHASTA MISC

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SYNC\_DATE=06/20/2005  
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SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE	SHT	OF
NONE	20	154

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## Page Notes

Power aliases required by this page:

```
- =PP3V3_PWRON_SB_PCI64 (VIO1) (TO 5V OR 3.3V)
```

```
- #PP3V3_PWRON_SB_PCI32 (VIO2) (TO 5V OR 3.3V)
```

```
- =PP3V3_PWRON_SB
```

```
- =PP2V5_PWRON_SB
```

```
- =PP1V2_PWRON_SB_VCORE
```

NOTE: PCI pads use the VIO supply to meet

different drive timing

characteristics required by the PCI

spec for 5V vs. 3.3V operation.

CONNECT VIO2 TO

appropriate PCI bus voltage and

VIO1 TO SAME IF 64-BIT

PCI, otherwise 3.3V.

Signal aliases required by this page:

( NONE )

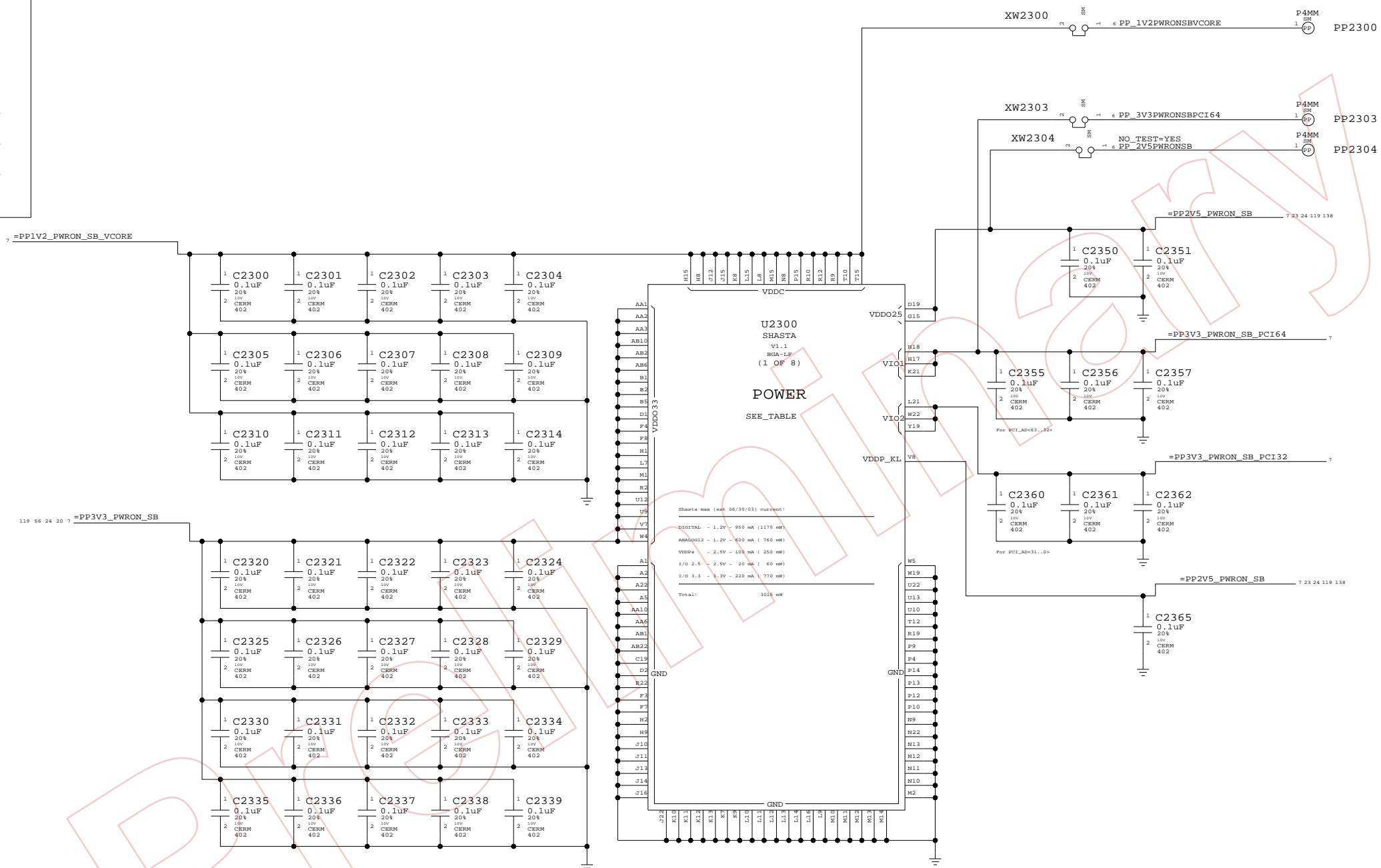
BOM options provided by this page:

( NONE )

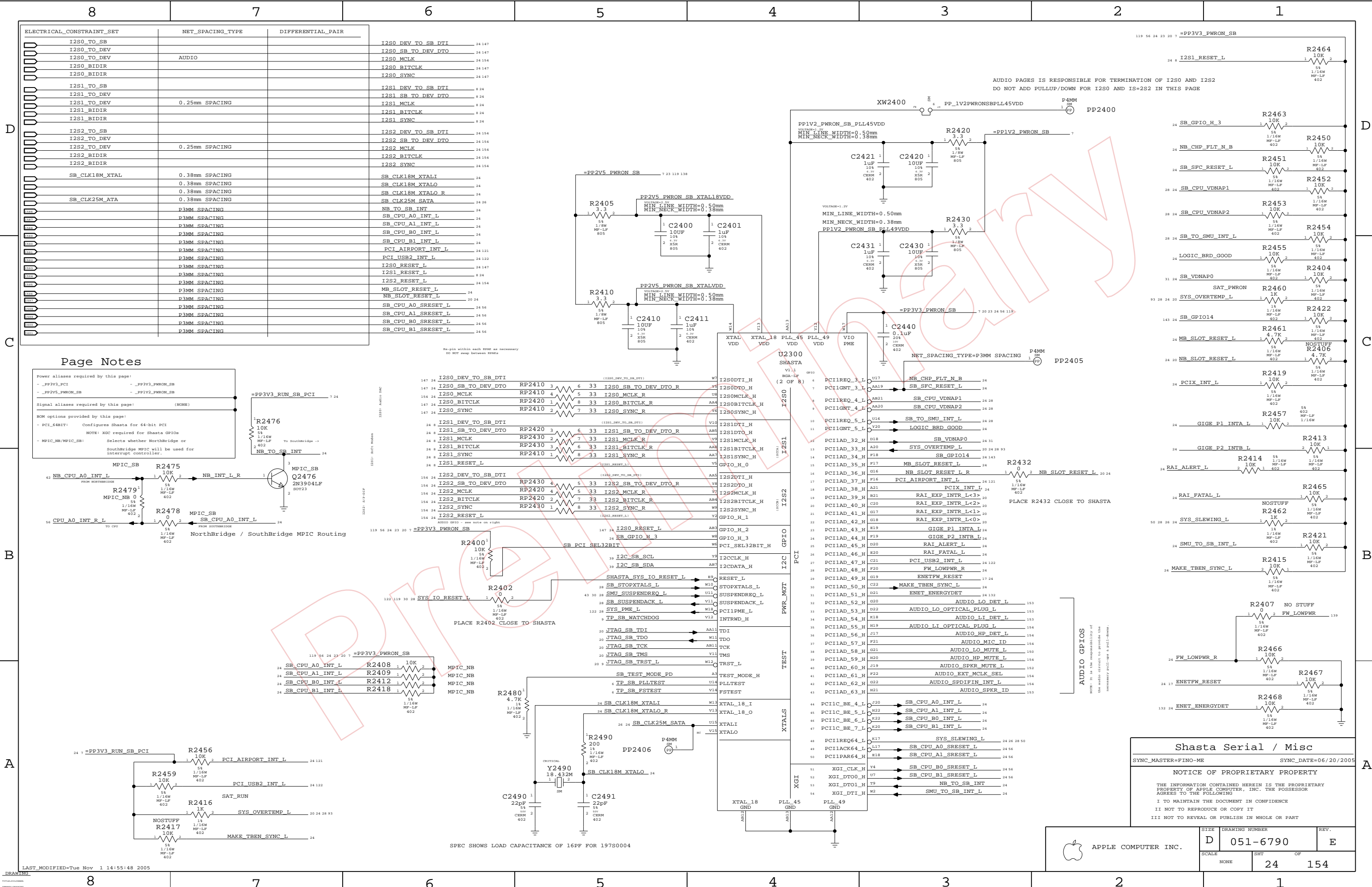
Power Sequencing:

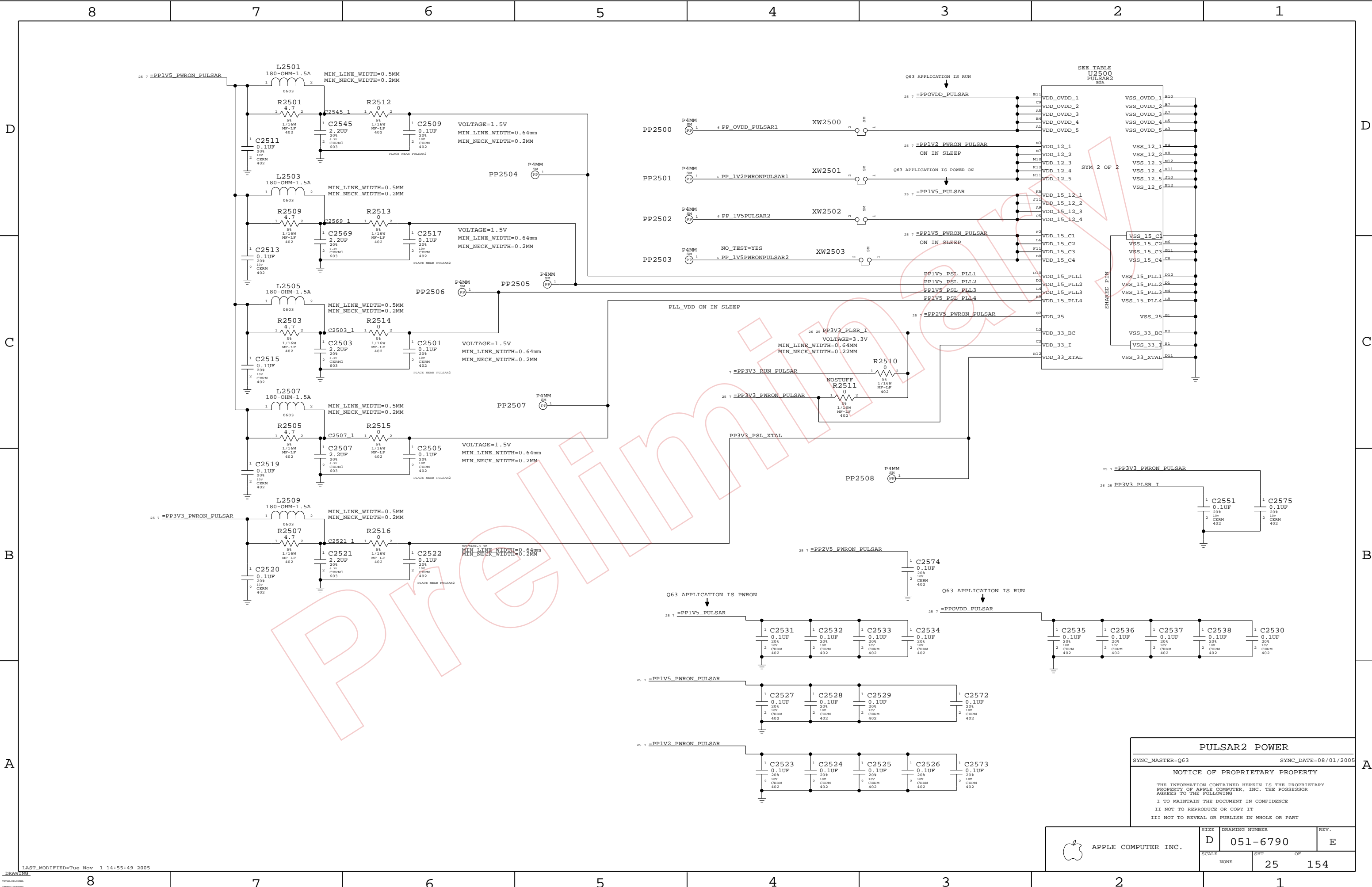
Must power Shasta VCore rail before any

other Shasta supplies.



Shasta Core Power	
SYNC_MASTER=Q63	SYNC_DATE=08/01/2005
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PULSAR2 POWER

SYNC\_MASTER=Q63

SYNC\_DATE=08/01/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	E
SCALE		SHT	OF
NONE		25	154







D

D

Page Notes

Power aliases required by this page:

- PP3V3\_ALL\_SMU
- PP3V3\_ALL\_RTC
- PP3V3\_PWRON\_SMU
- PPVREF\_SMU (SMU AVCC OR 2.5V REFERENCE)

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

NOTE: CPU current/voltage monitoring (CPU\_SENSE\_I/CPU\_SENSE\_V) requires 100K/10uF RC filter at SMU pins. Caps should connect to GND\_SMU\_AVSS. SMU\_VREF should be same signal or reference used by monitoring circuit, but be aware that this will affect other analog inputs such as AC adapter ID.

NOTE: All analog inputs to SMU should have a 100pF capacitor to the SMU AVSS signal (GND\_SMU\_AVSS). None of those capacitors are provided on this page.

NOTE: Some primary and alternate functions require pull-ups that are not provided on this page. Please review the latest SMU specification to ensure missing pull-ups are provided on another page.

NOTE: Pinout matches SMU pinout v1.51.

C

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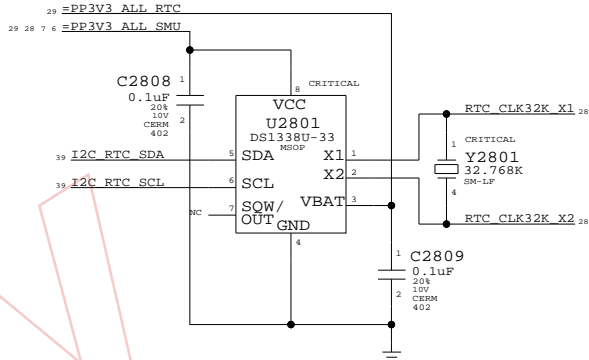
A

Alternate Functions

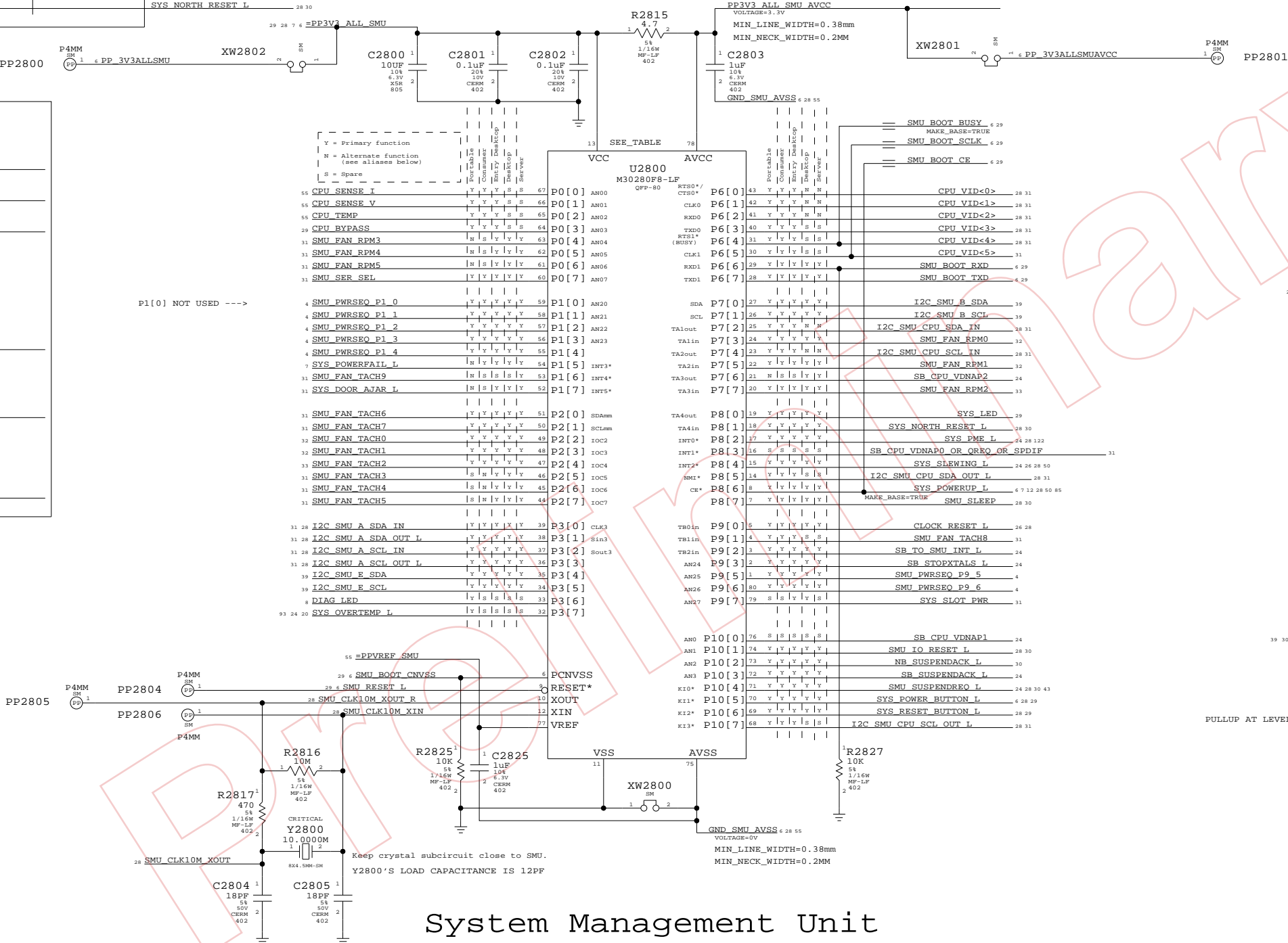
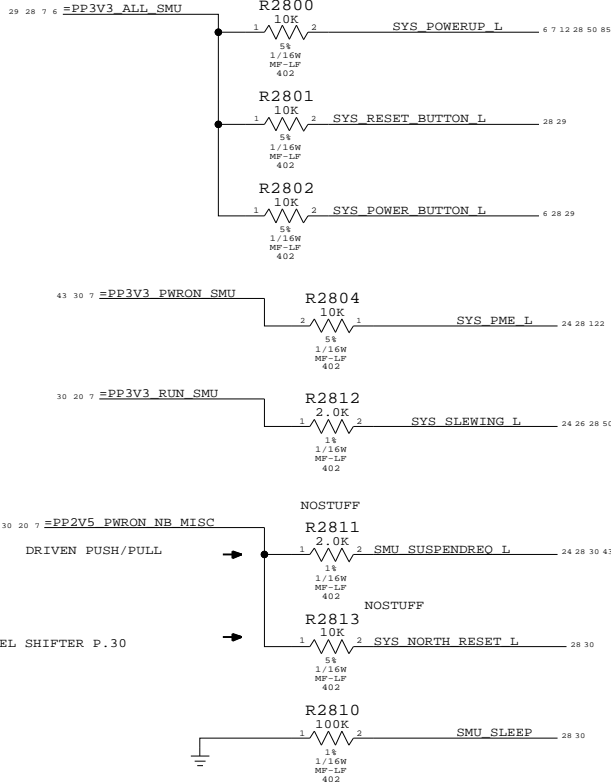
System Management Unit

Tower & Server			
Port		Port	
31 28 CPU VID<0>	6.0	SAT MRESET L	
31 28 CPU VID<1>	6.1	CPU A INSERTED L	
31 28 CPU VID<2>	6.2	CPU B INSERTED L	
31 28 I2C SMU CPU SDA IN	7.3	SMU FAN PWM8	
31 28 I2C SMU CPU SCL IN	7.4	SMU FAN PWM9	
31 28 I2C SMU A SDA IN	3.0	I2C SMU A SDA	31 39
31 28 I2C SMU A SDA OUT L	3.1	I2C SMU A SCL	31 39

Real Time Clock



SMU Pull-ups / pull-down



System Management Unit

SYNC\_MASTER=Q63

SYNC\_DATE=08/01/2005

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SIZE

D

DRAWING NUMBER

051-6790

REV.

E

SCALE

NONE

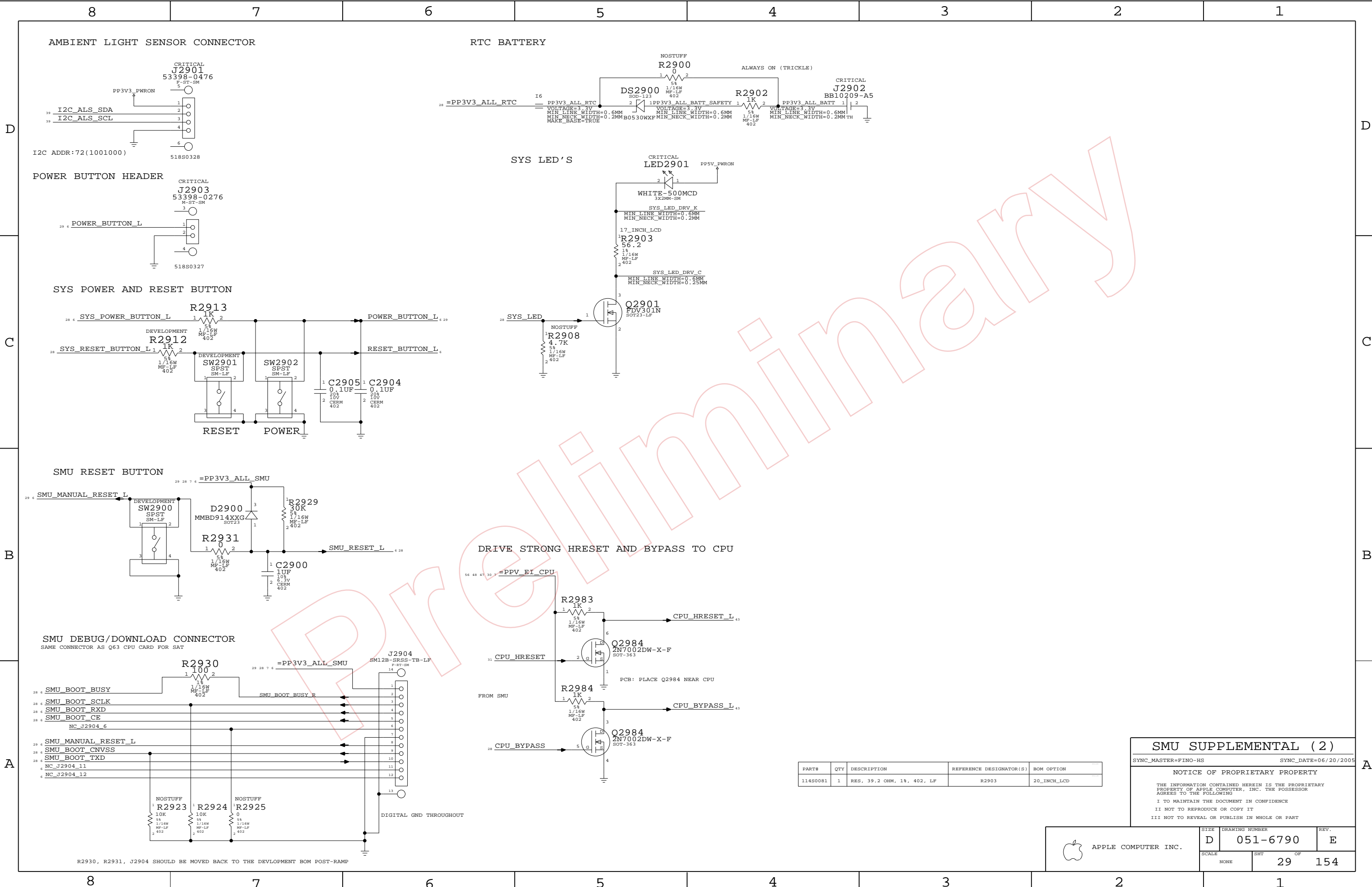
SHT

28

OF

154

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0081	1	RES, 39.2 OHM, 1%, 402, LF	R2903	20_INCH_LCD

SMU SUPPLEMENTAL ( 2 )

SYNC\_MASTER=FINO-HS

SYNC\_DATE=06/20/2005

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APPLE COMPUTER INC.

SCALE  
NONE

D

DRAWING NUMBER  
051-6790

SHT  
29

REV.  
E

OF  
154





8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

SMII ALIASES	PF3V3 RUN
--------------	-----------

USFO RELEASED  
ALIASES ARE ONLY NECESSARY WHERE USE DIFFERS FROM Q63.

COMMENT (ONLY IF USE DIFFERS FROM Q63)	M23 NET NAME	M23 SMU ALLOCATION	Q63 NET NAME (SHARED PAGE)

[illegible][illegible]

M23/M33 DOESN'T HAVE THOSE FANS.	NC SMU FAN RPM4	FAN_CNTL0_5	MAKE_BASE=TRUE	SMU FAN RPM4	28
	NC SMU FAN RPM5	FAN_CNTL0_6	MAKE_BASE=TRUE	SMU FAN RPM5	28
		PU 6			28

28	CPU VID <0>	MAKE_BASE=TRUE	1	0	2	CPU VID R<0>	50

Q63 USES SMU\_SER\_SEL FOR SPDIF-SMU-DEBUG. NOT M23/M33 FEATURE. NC SMU\_SER\_SEL SMU\_SER\_SEL 28

SMU USES P1.1, P1.2, P1.3, P9.5, P9.6 FOR PWRSEQ ON PG 7.	CPU_SENSE_V1 P1.1 CPU_TEMP1 P1.2		CPU_VID<2>
---	---	--	------------

M23/M33 DOESN'T USE P1.4. NC ON PG 7.

P1\_1 P1.3  
P1\_4 P1.4  
POWERFAIL\* P1.5

28 CPU VID<3> R3.022 1/15W 402 1 1 2 CPU VID R<3>

MAKE BASETHRU

CPU_VID_L0 FOR Q82, NOT M2M/M33 FEATURE	NC_SMU_CPU_VID_L0	CPU_VID_L0	D1_6	SMU_FAN_TACH9	28
CONSIDER DOOR_AJAR FOR M2M/M33 DIMM ACCESS DOOR?	NC_SYS_DOOR_AJAR_L	DOOR_AJAR*	MAX_SANITY_T	SYS_DOOR_AJAR_L	28
			1		28
			2		28
			3		28
			4		28
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			91		28
		</			

[illegible]

Diagram illustrating the pin connections for the M23/M33 module, showing various signals and their connections to the CPU and other components.

**Pin Connections:**

- NC SMU FAN TACH3** (P2.5) connects to **SMU FAN TACH3** (P2.5).
- NC SMU FAN TACH4** (P2.6) connects to **SMU FAN TACH4** (P2.6).
- NC SMU FAN TACH5** (P2.7) connects to **SMU FAN TACH5** (P2.7).
- I2C SMU A SDA** (P2.8) connects to **I2C SMU A SDA IN** (P2.8).
- I2C SMU A SCL** (P2.9) connects to **I2C SMU A SCL OUT L** (P2.9).
- SMU JTAG TDI** (P2.10) connects to **I2C SMU A SCL IN** (P2.10).
- SMU JTAG TCK** (P2.11) connects to **I2C SMU A SCL OUT L** (P2.11).
- IIC\_E\_DAT** (P3.4) connects to **I2C SMU CPU SDA IN** (P7.2).
- IIC\_E\_CLK** (P3.5) connects to **I2C SMU CPU SCL IN** (P7.4).
- DIAG\_LED** (P3.6) connects to **I2C SMU CPU SCL IN** (P7.4).
- OVERTEMP\*** (P3.7) connects to **I2C SMU CPU SCL IN** (P7.4).
- CPU\_VID[0]** (P6.0) connects to **I2C SMU CPU SCL IN** (P7.4).
- CPU\_VID[1]** (P6.1) connects to **I2C SMU CPU SCL IN** (P7.4).
- CPU\_VID[2]** (P6.2) connects to **I2C SMU CPU SCL IN** (P7.4).
- CPU\_VID[3]** (P6.3) connects to **I2C SMU CPU SCL IN** (P7.4).
- CPU\_VID[4]** (P6.4) connects to **I2C SMU CPU SCL IN** (P7.4).
- CPU\_VID[5]** (P6.5) connects to **I2C SMU CPU SCL IN** (P7.4).
- DEBUG\_RXD** (P6.6) connects to **I2C SMU CPU SCL IN** (P7.4).
- DEBUG\_TXD** (P6.7) connects to **I2C SMU CPU SCL IN** (P7.4).
- IIC\_B\_DAT** (P7.0) connects to **I2C SMU CPU SCL IN** (P7.4).
- IIC\_B\_CLK** (P7.1) connects to **I2C SMU CPU SCL IN** (P7.4).
- SMU CPU NB\_SEL** (P7.2) connects to **I2C SMU CPU SDA IN** (P7.2).
- NC I2C SMU CPU SCL\_IN** (P7.4) connects to **I2C SMU CPU SCL IN** (P7.4).
- FAN\_CNTL7\_3** (P7.3) connects to **I2C SMU CPU SCL IN** (P7.4).
- FAN\_CNTL7\_4** (P7.4) connects to **I2C SMU CPU SCL IN** (P7.4).
- FAN\_CNTL7\_5** (P7.5) connects to **I2C SMU CPU SCL IN** (P7.4).
- VDNAP2** (P7.6) connects to **I2C SMU CPU SCL IN** (P7.4).
- FAN\_CNTL7\_7** (P7.7) connects to **I2C SMU CPU SCL IN** (P7.4).
- SYSTEM\_LED** (P8.0) connects to **I2C SMU CPU SCL IN** (P7.4).
- NB\_RESET\*** (P8.1) connects to **I2C SMU CPU SCL IN** (P7.4).
- PME\*** (P8.2) connects to **I2C SMU CPU SCL IN** (P7.4).
- VDNAP0** (P8.3) connects to **SB CPU VDNAP0 OR QREQ OR SPDIF** (P8.3).
- SLEWING\*** (P8.4) connects to **SB CPU VDNAP0 OR QREQ OR SPDIF** (P8.3).
- NR\_TMS** (P8.5) connects to **I2C SMU CPU SDA OUT L** (P8.5).
- POWERUP\*** (P8.6) connects to **I2C SMU CPU SDA OUT L** (P8.5).
- SLEEP** (P8.7) connects to **I2C SMU CPU SDA OUT L** (P8.5).
- CLK\_RESET\*** (P8.8) connects to **I2C SMU CPU SDA OUT L** (P8.5).
- CPU HRESET** (P9.1) connects to **SMU FAN TACH8** (P9.1).
- SMU DOORBELL\*** (P9.2) connects to **SMU FAN TACH8** (P9.1).
- STOP\_XTAL\*** (P9.3) connects to **SMU FAN TACH8** (P9.1).
- PS9\_5** (P9.5) connects to **SMU FAN TACH8** (P9.1).
- PS9\_6** (P9.6) connects to **SMU FAN TACH8** (P9.1).
- NC SLOT TOTAL PWR** (P9.7) connects to **SYS SLOT PWR** (P9.7).
- VDNAP1** (P10.0) connects to **SYS SLOT PWR** (P9.7).
- IO\_RESET\*** (P10.1) connects to **SYS SLOT PWR** (P9.7).
- SUSPEND\_ACK\*** (P10.2) connects to **SYS SLOT PWR** (P9.7).
- SUSPEND\_IO\_ACK\*** (P10.3) connects to **SYS SLOT PWR** (P9.7).
- SUSPEND\_REQ\*** (P10.4) connects to **SYS SLOT PWR** (P9.7).
- PWR\_BUTTON\*** (P10.5) connects to **SYS SLOT PWR** (P9.7).
- RST\_BUTTON\*** (P10.6) connects to **SYS SLOT PWR** (P9.7).
- SMU JTAG TDO** (P10.7) connects to **I2C SMU CPU SCL OUT L** (P10.7).
- TDO** (P10.7) connects to **I2C SMU CPU SCL OUT L** (P10.7).

**Notes:**

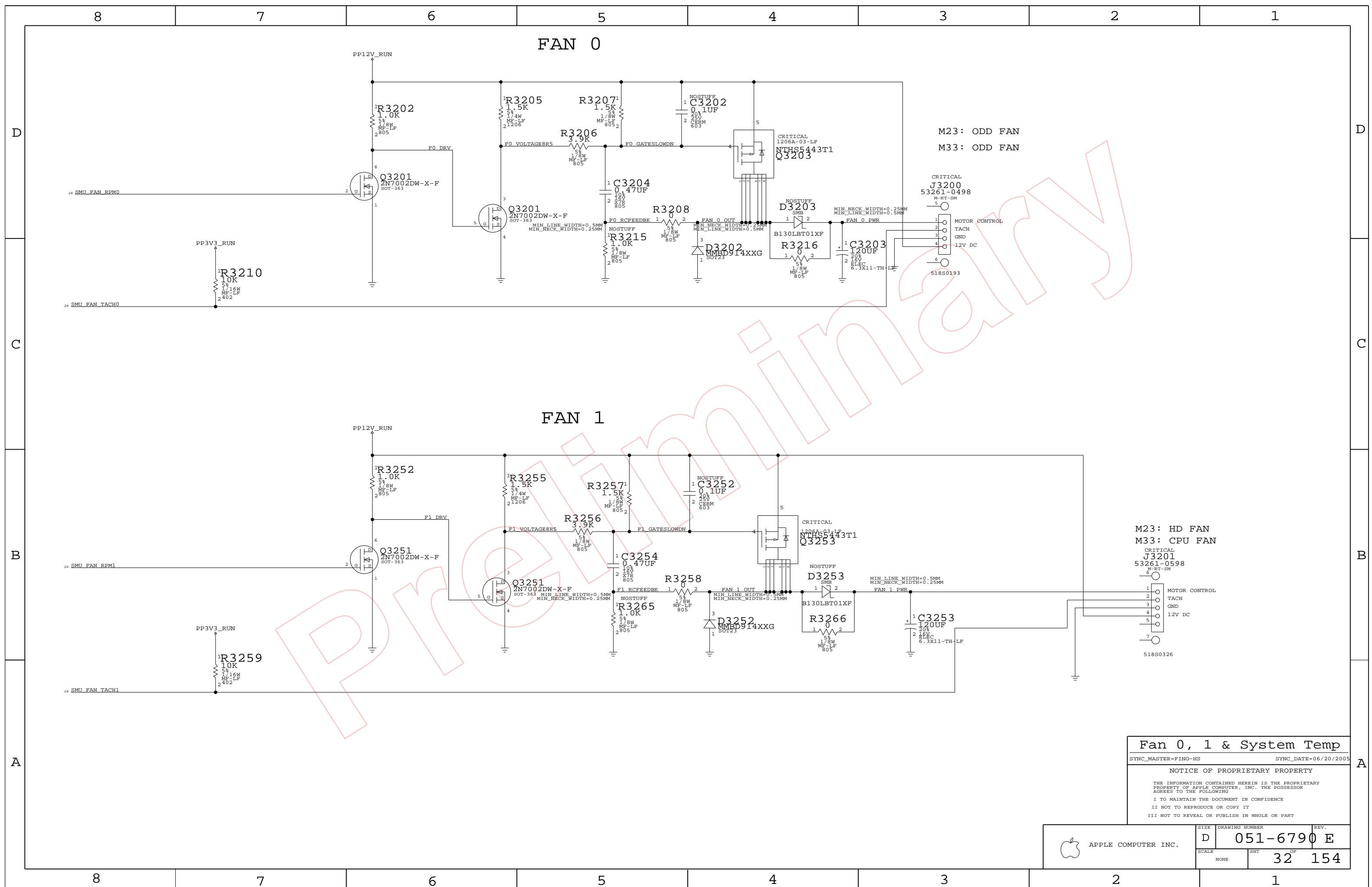
- M23/M33 DOESN'T HAVE FAN TACHS P2.5, P2.6, P2.7. M23/M33 USES TACH0 (P2.2), TACH1 (P2.3), TACH2 (P2.4) ONLY.
- M23/M33 ONLY CONNECTS I2C TO KODIAK NOW; CPU HAS PULLUPS ON ITS PG.
- Q63 USE OF P7.2 IS PWM FAN SELECT BETWEEN CPU OR NB TMS AND TDO FROM/TO SMU
- M23/M33 DOESN'T HAVE THIS FAN (P7.4) M23/M33 USES FAN\_RPM0 (P7.3), FAN\_RPM1 (P7.5), FAN\_RPM2 (P7.7) ONLY.
- M23/M33 DOESN'T NEED TO MAKE VDNAP0 DO TRIPLE-DUTY.
- Q63 USE OF P9.1 IS TACH 8.
- SMU USES P1.1, P1.2, P1.3, P9.5, P9.6 FOR PWRSEQ ON PG 7.
- M23/M33 HAS NO SLOTS.

**Pin Connections (continued):**

- NC SMU FAN TACH3** (P2.5) connects to **SMU FAN TACH3** (P2.5).
- NC SMU FAN TACH4** (P2.6) connects to **SMU FAN TACH4** (P2.6).
- NC SMU FAN TACH5** (P2.7) connects to **SMU FAN TACH5** (P2.7).
- I2C SMU A SDA** (P2.8) connects to **I2C SMU A SDA IN** (P2.8).
- I2C SMU A SCL** (P2.9) connects to **I2C SMU A SCL OUT L** (P2.9).
- SMU JTAG TDI** (P2.10) connects to **I2C SMU A SCL IN** (P2.10).
- SMU JTAG TCK** (P2.11) connects to **I2C SMU A SCL OUT L** (P2.11).
- IIC\_E\_DAT** (P3.4) connects to **I2C SMU CPU SDA IN** (P7.2).
- IIC\_E\_CLK** (P3.5) connects to **I2C SMU CPU SCL IN** (P7.4).
- DIAG\_LED** (P3.6) connects to **I2C SMU CPU SCL IN** (P7.4).
- OVERTEMP\*** (P3.7) connects to **I2C SMU CPU SCL IN** (P7.4).
- CPU\_VID[0]** (P6.0) connects to **I2C SMU CPU SCL IN** (P7.4).
- CPU\_VID[1]** (P6.1) connects to **I2C SMU CPU SCL IN** (P7.4).
- CPU\_VID[2]** (P6.2) connects to **I2C SMU CPU SCL IN** (P7.4).
- CPU\_VID[3]** (P6.3) connects to **I2C SMU CPU SCL IN** (P7.4).
- CPU\_VID[4]** (P6.4) connects to **I2C SMU CPU SCL IN** (P7.4).
- CPU\_VID[5]** (P6.5) connects to **I2C SMU CPU SCL IN** (P7.4).
- DEBUG\_RXD** (P6.6) connects to **I2C SMU CPU SCL IN** (P7.4).
- DEBUG\_TXD** (P6.7) connects to **I2C SMU CPU SCL IN** (P7.4).
- IIC\_B\_DAT** (P7.0) connects to **I2C SMU CPU SCL IN** (P7.4).
- IIC\_B\_CLK** (P7.1) connects to **I2C SMU CPU SCL IN** (P7.4).
- SMU CPU NB\_SEL** (P7.2) connects to **I2C SMU CPU SDA IN** (P7.2).
- NC I2C SMU CPU SCL\_IN** (P7.4) connects to **I2C SMU CPU SCL IN** (P7.4).
- FAN\_CNTL7\_3** (P7.3) connects to **I2C SMU CPU SCL IN** (P7.4).
- FAN\_CNTL7\_4** (P7.4) connects to **I2C SMU CPU SCL IN** (P7.4).
- FAN\_CNTL7\_5** (P7.5) connects to **I2C SMU CPU SCL IN** (P7.4).
- VDNAP2** (P7.6) connects to **I2C SMU CPU SCL IN** (P7.4).
- FAN\_CNTL7\_7** (P7.7) connects to **I2C SMU CPU SCL IN** (P7.4).
- SYSTEM\_LED** (P8.0) connects to **I2C SMU CPU SCL IN** (P7.4).
- NB\_RESET\*** (P8.1) connects to **I2C SMU CPU SCL IN** (P7.4).
- PME\*** (P8.2) connects to **I2C SMU CPU SCL IN** (P7.4).
- VDNAP0** (P8.3) connects to **SB CPU VDNAP0 OR QREQ OR SPDIF** (P8.3).
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- NR\_TMS** (P8.5) connects to **I2C SMU CPU SDA OUT L** (P8.5).
- POWERUP\*** (P8.6) connects to **I2C SMU CPU SDA OUT L** (P8.5).
- SLEEP** (P8.7) connects to **I2C SMU CPU SDA OUT L** (P8.5).
- CLK\_RESET\*** (P8.8) connects to **I2C SMU CPU SDA OUT L** (P8.5).
- CPU HRESET** (P9.1) connects to

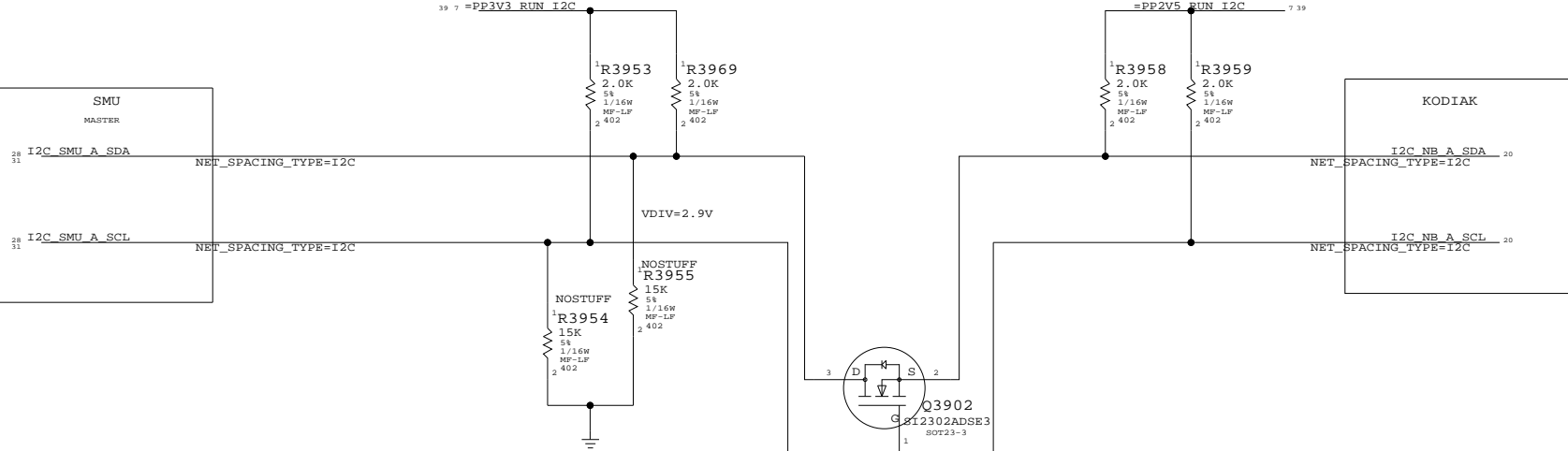


8	7	6	5	4	3	2	1
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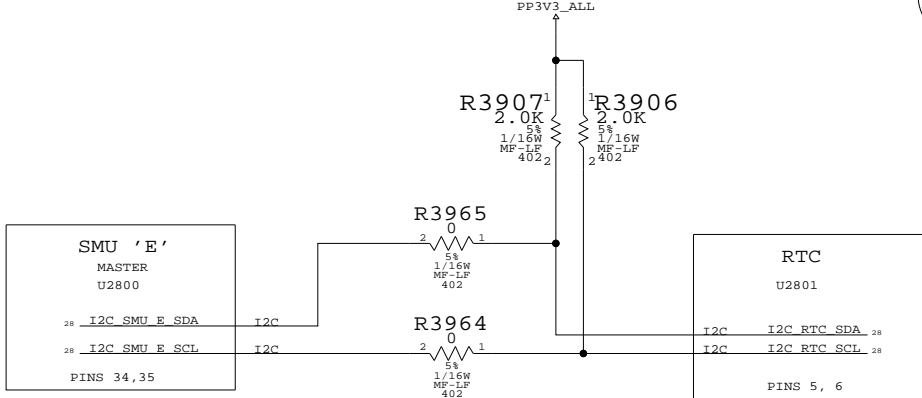




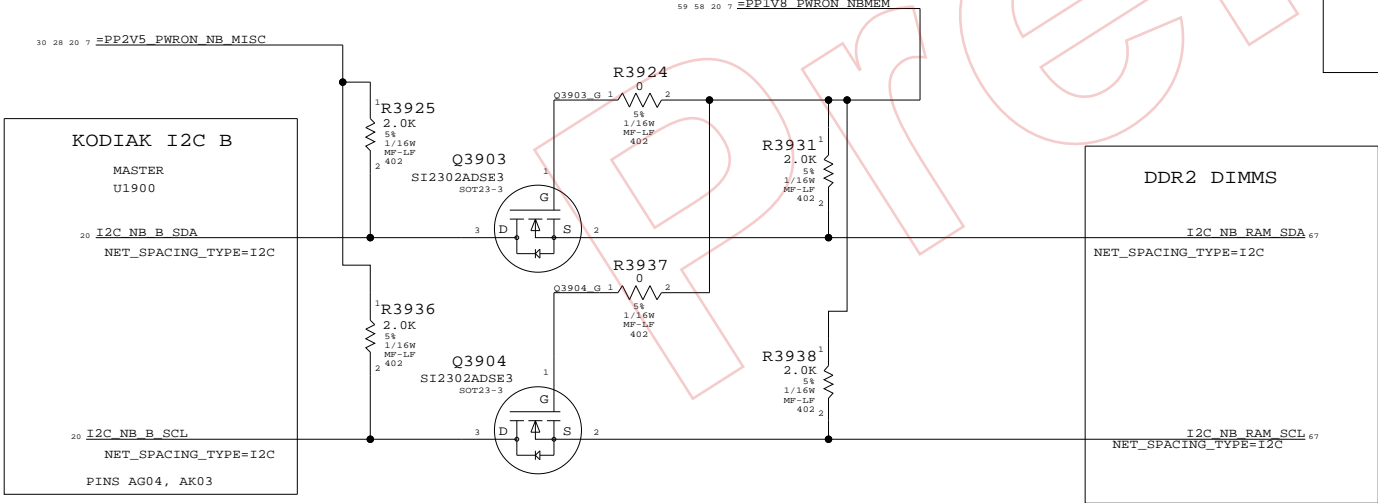
SMU AND NB I2C A BUS



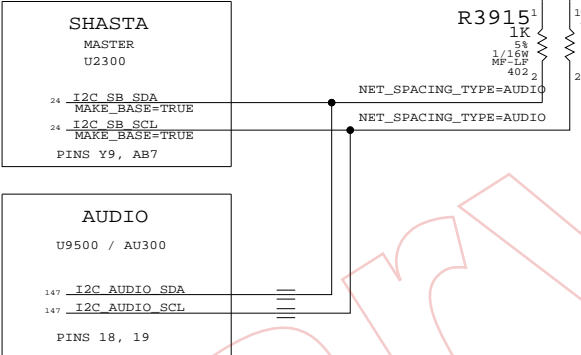
SMU I2C E BUS



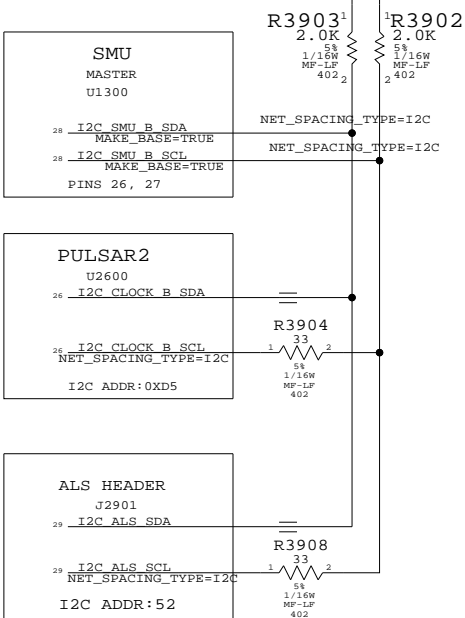
NB I2C B BUS



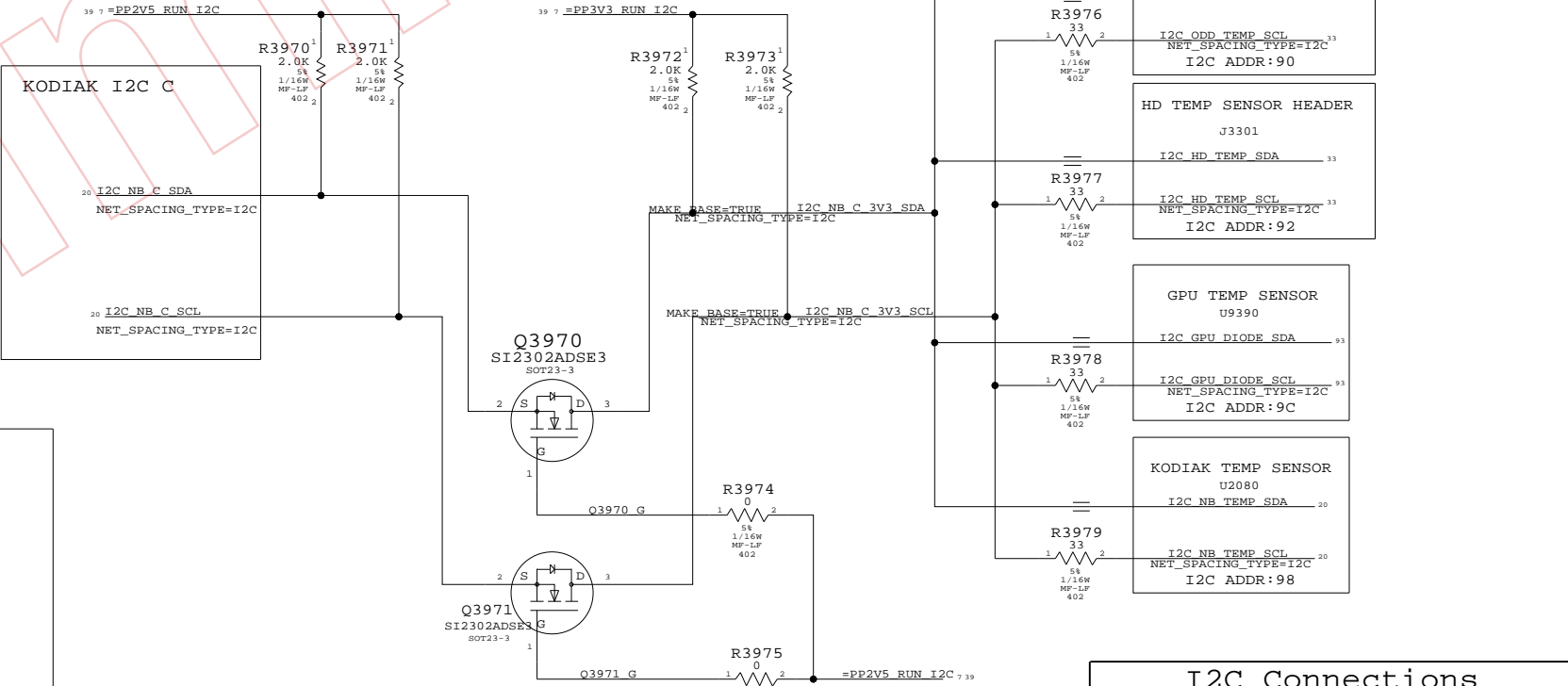
SB I2C BUS



SMU I2C B BUS



NB I2C C BUS



I2C Connections

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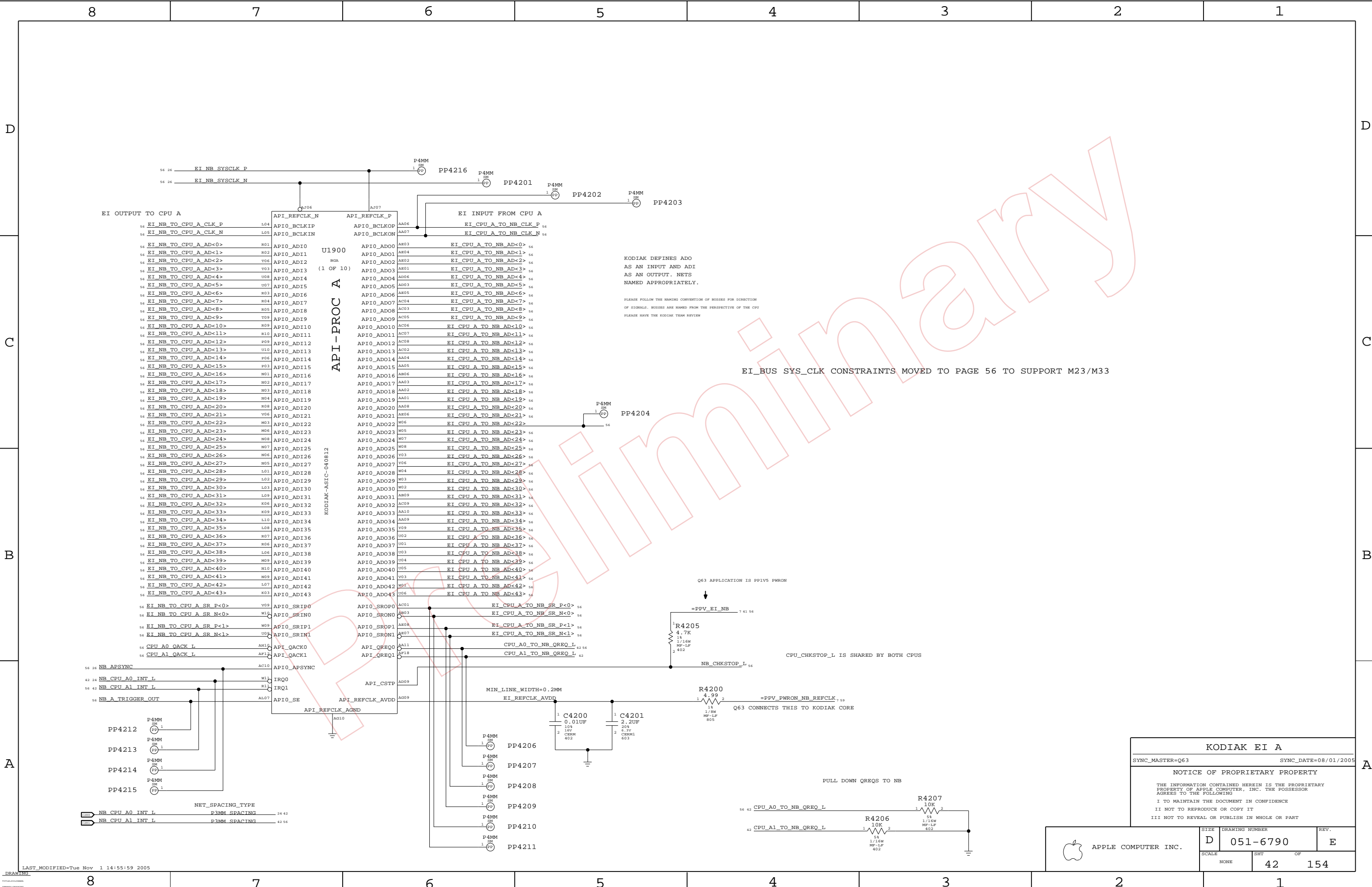


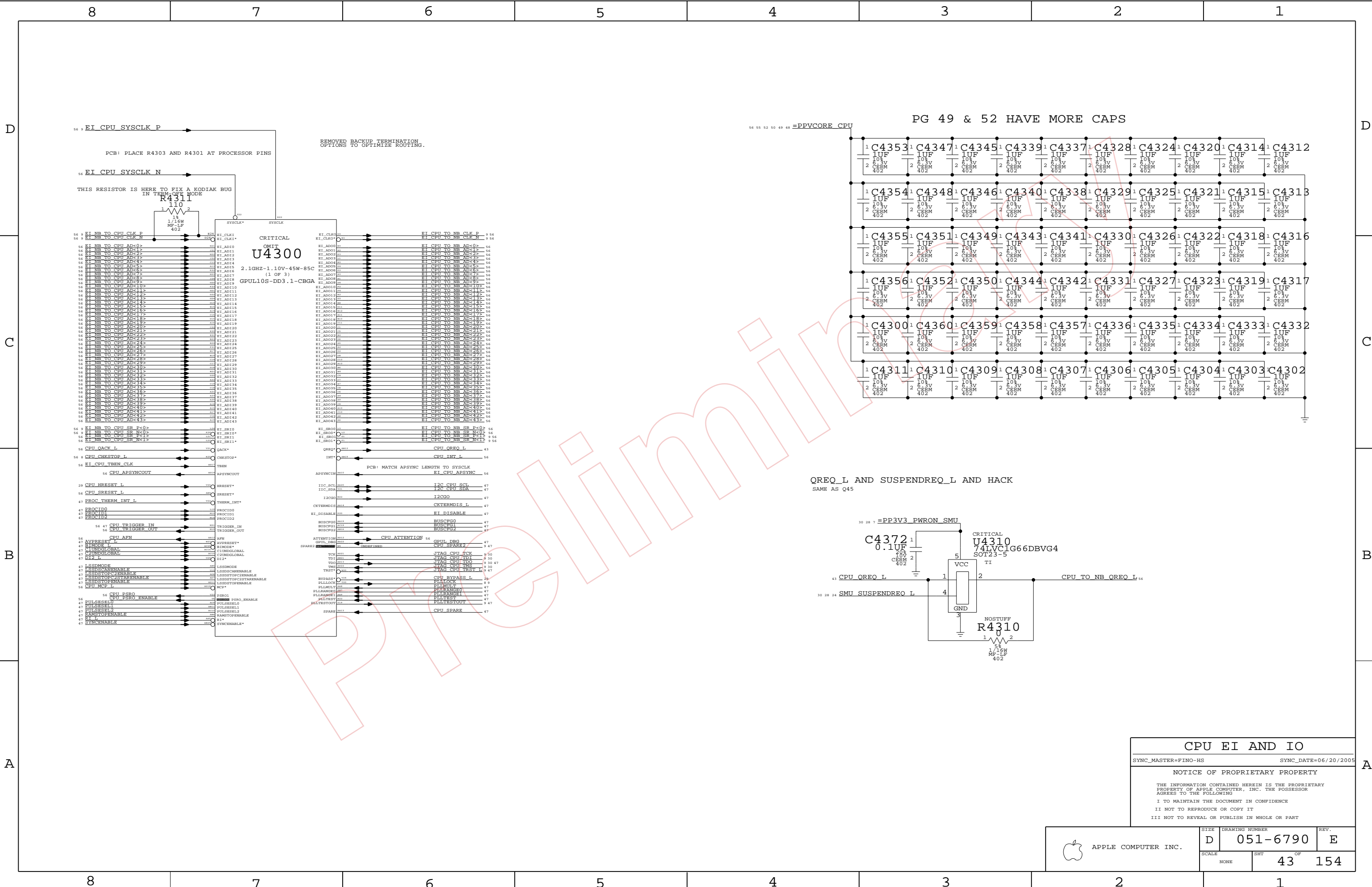
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SCALE	SHT	
NONE	39 <sup>OF</sup>	154









CPU EI AND IO

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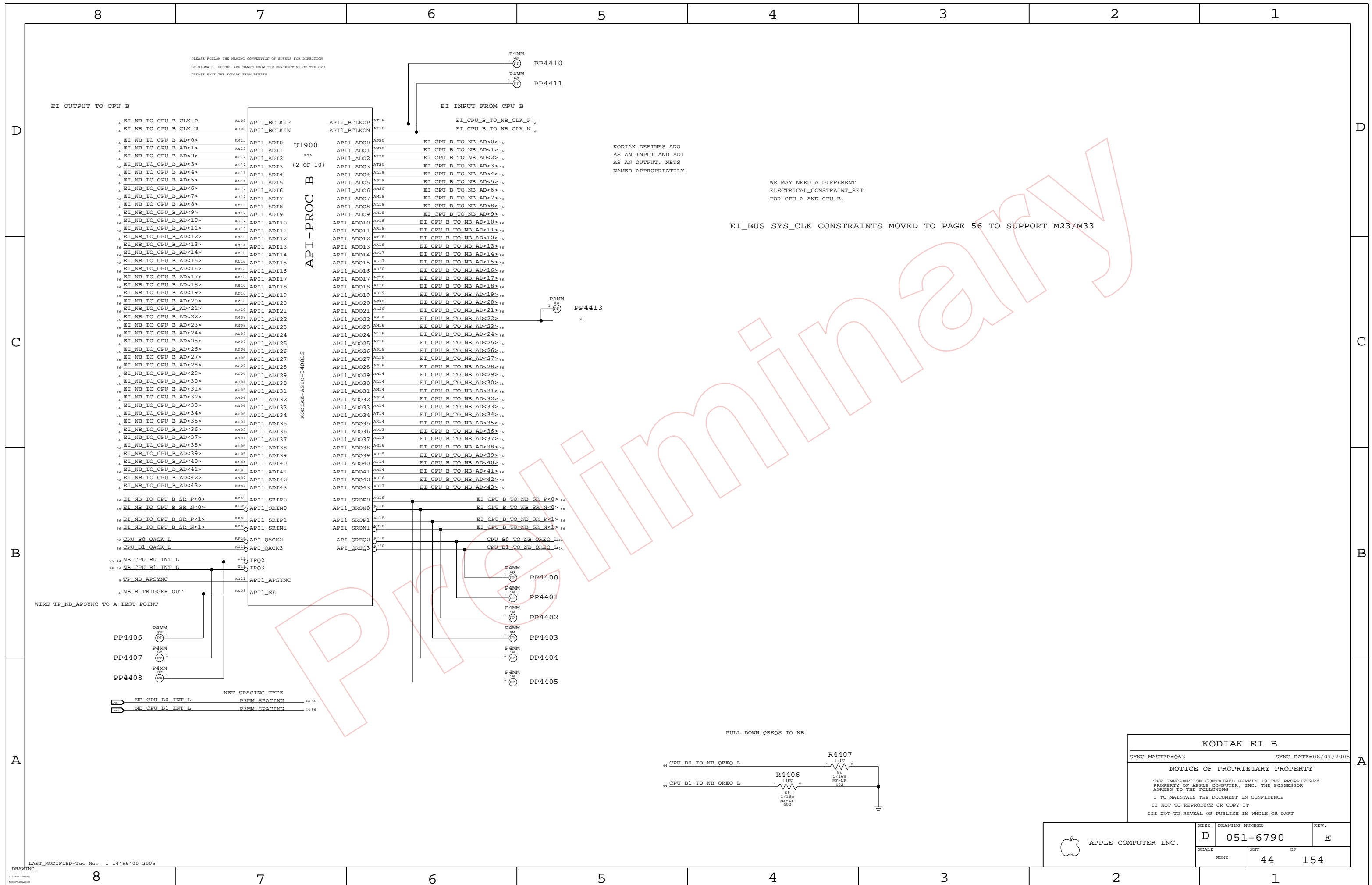
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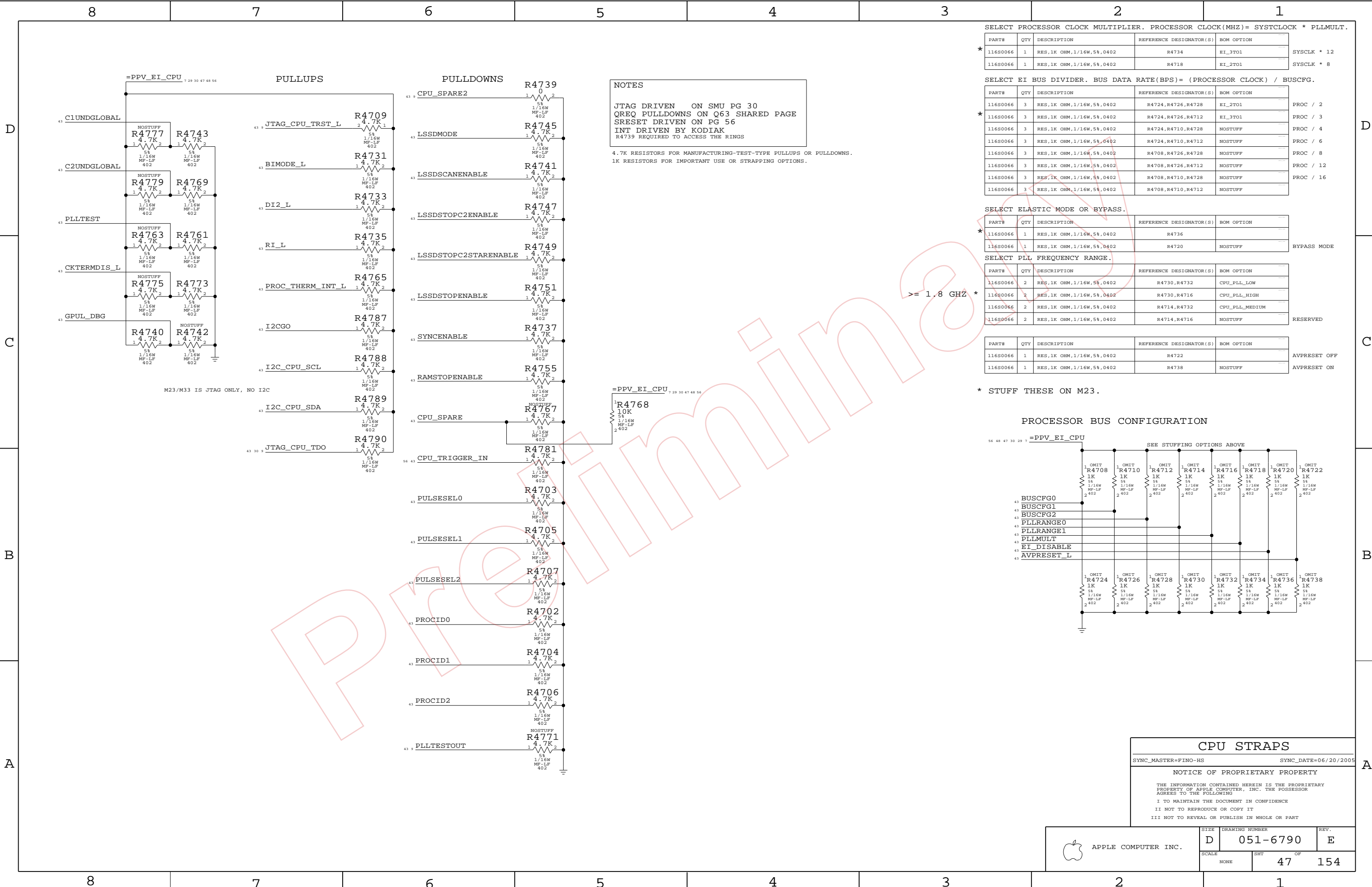
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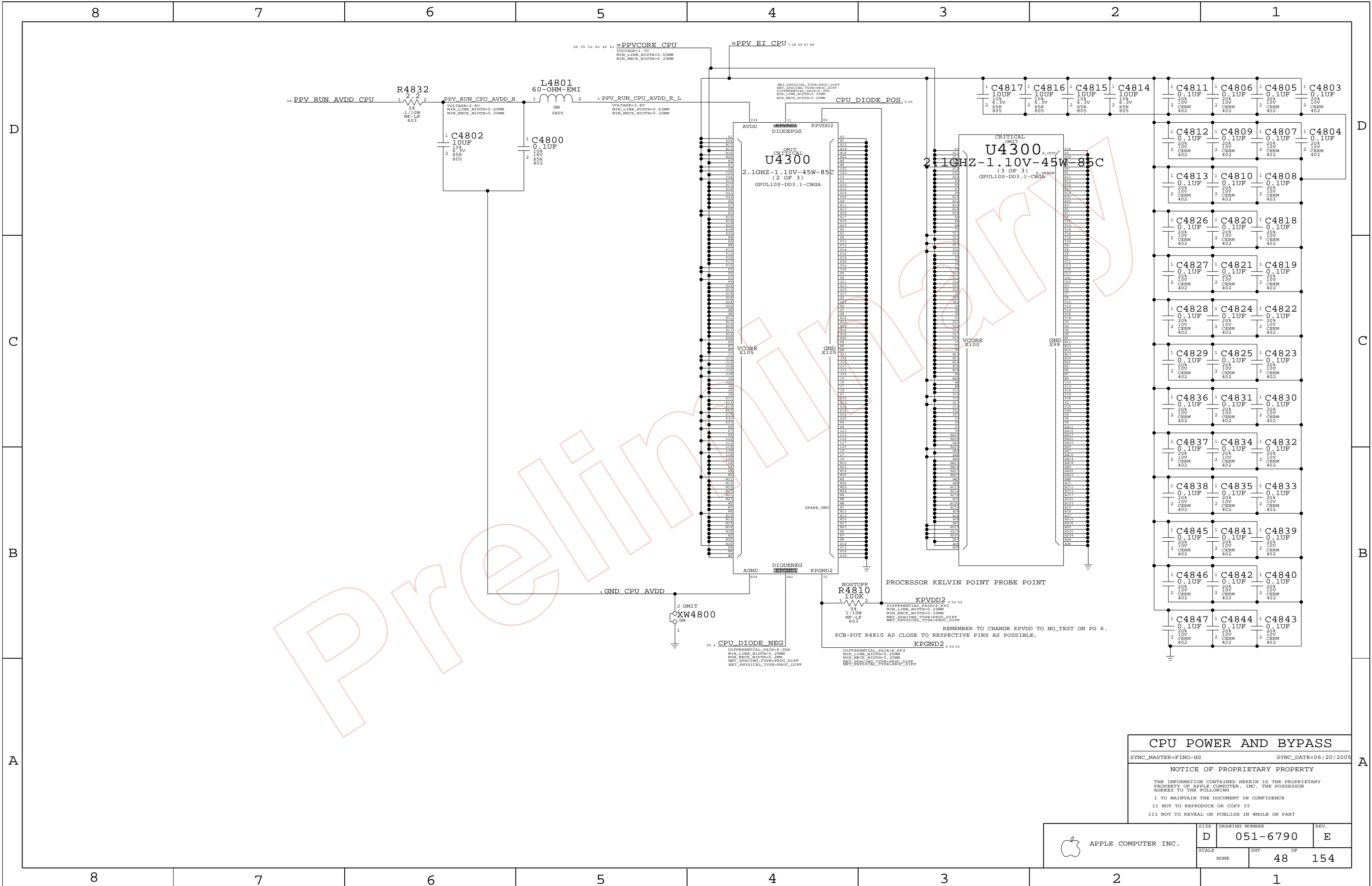
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CPU POWER AND BYPASS

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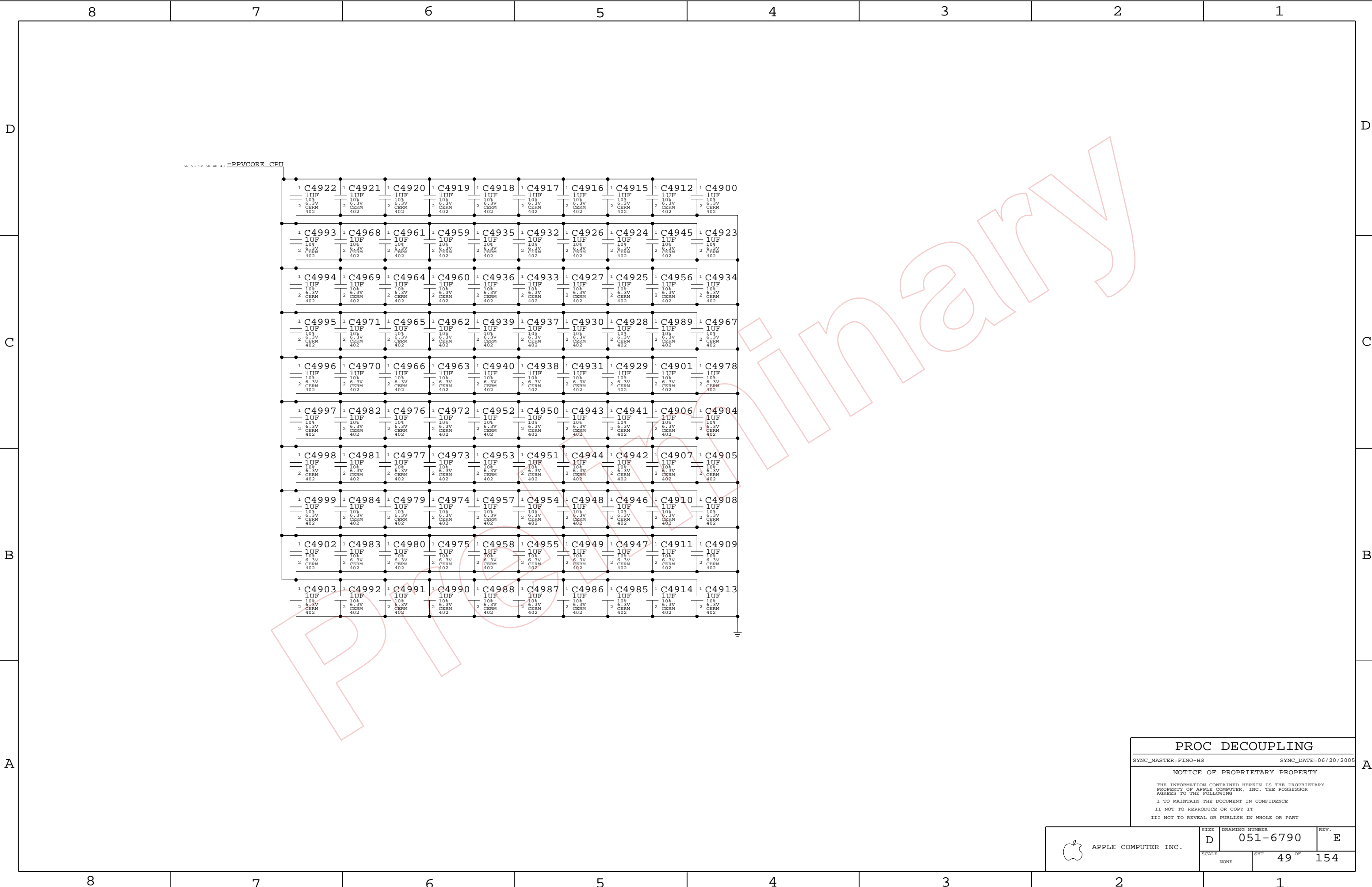
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PROC DECOUPLING

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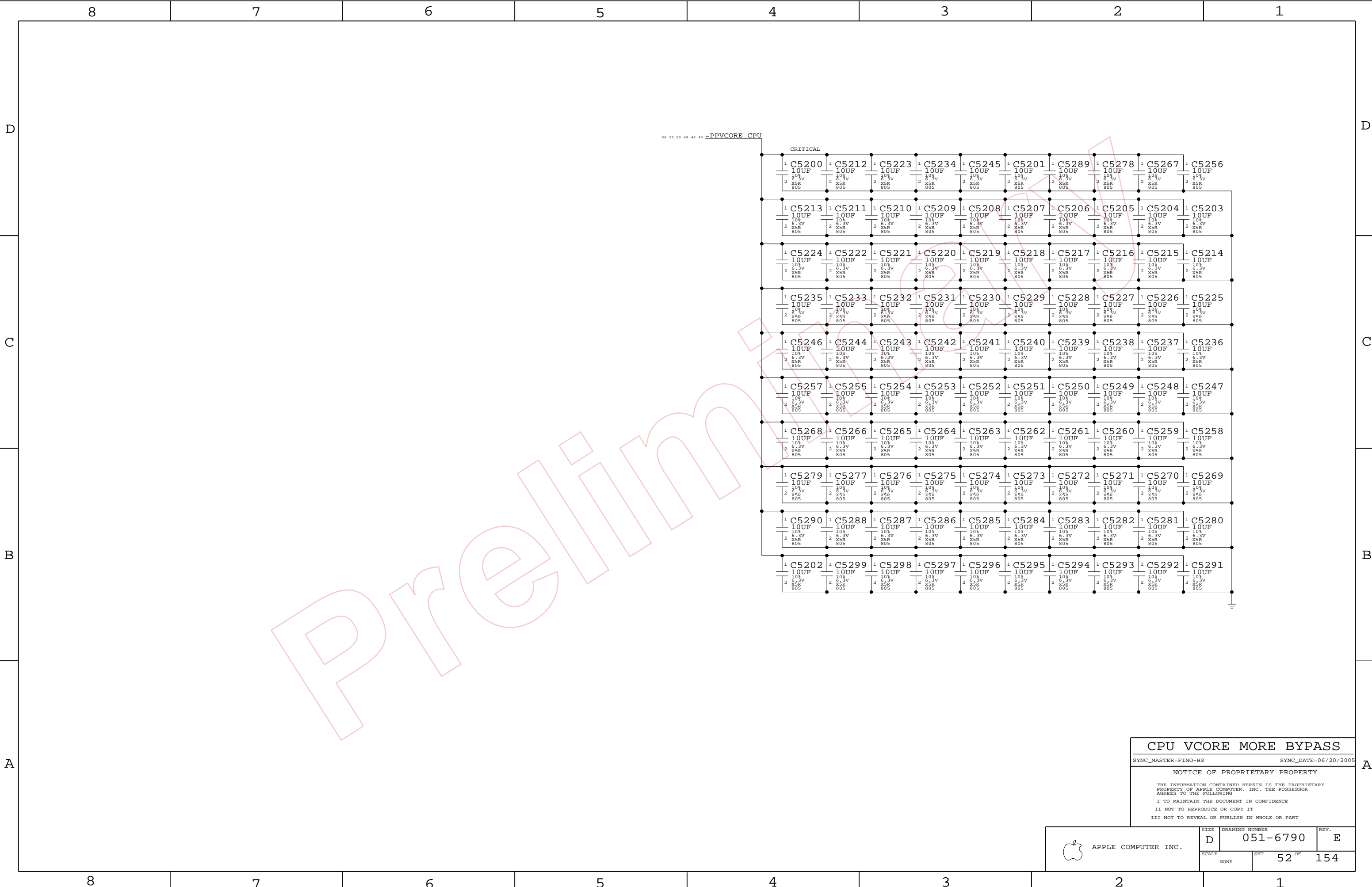
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CPU VCORE MORE BYPASS

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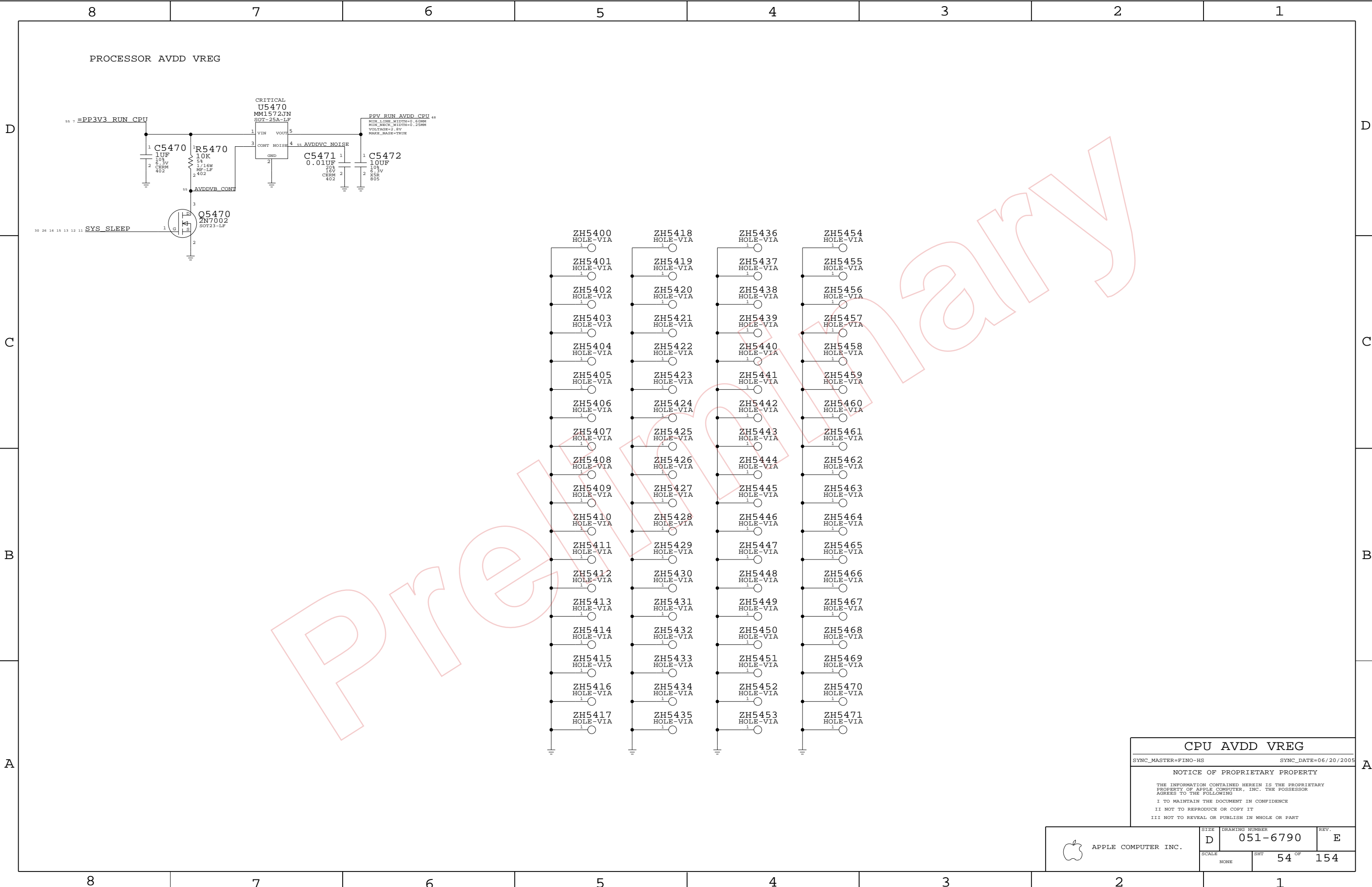
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	NONE	52 OF 154	



CPU AVDD VREG

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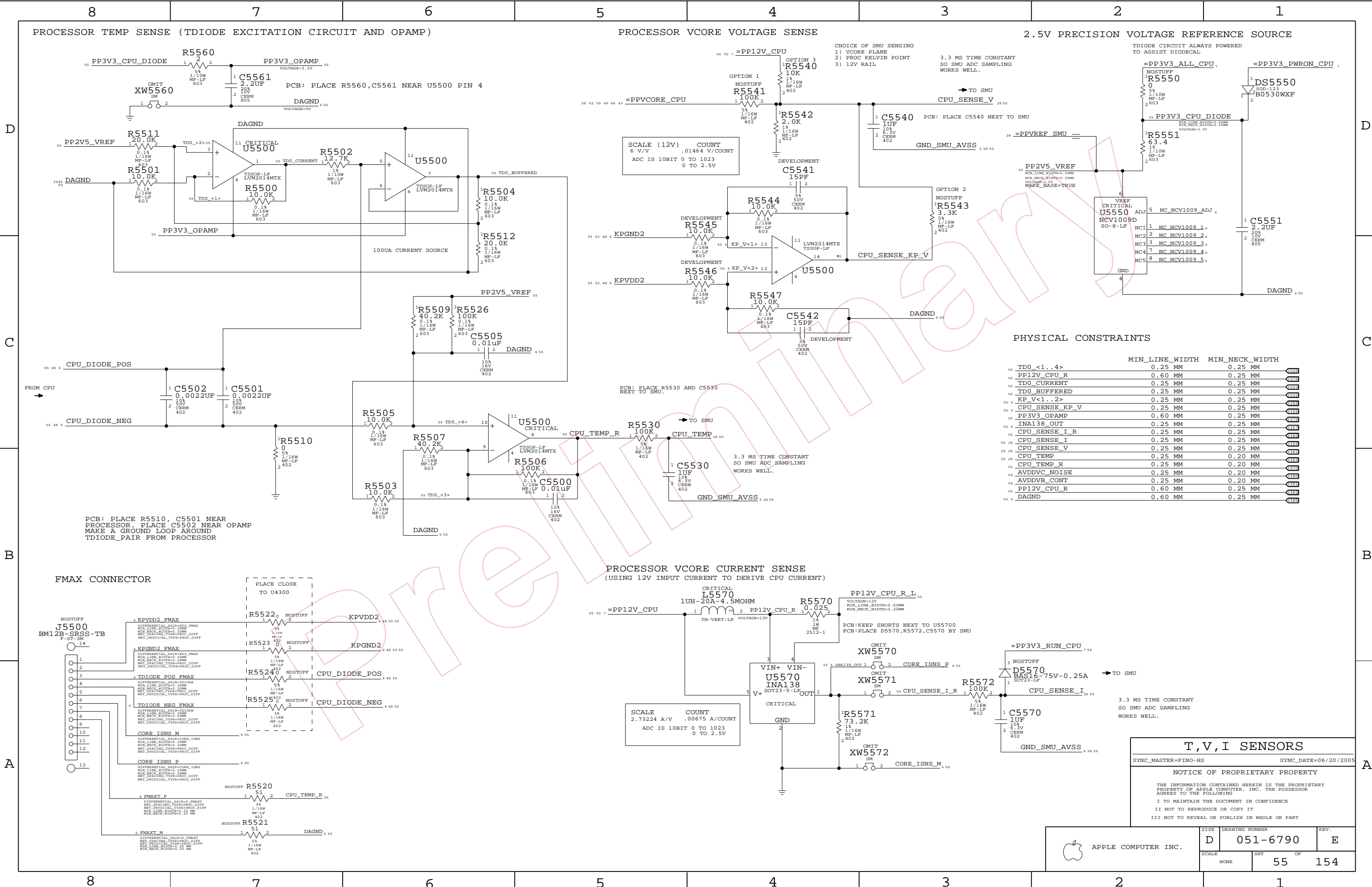
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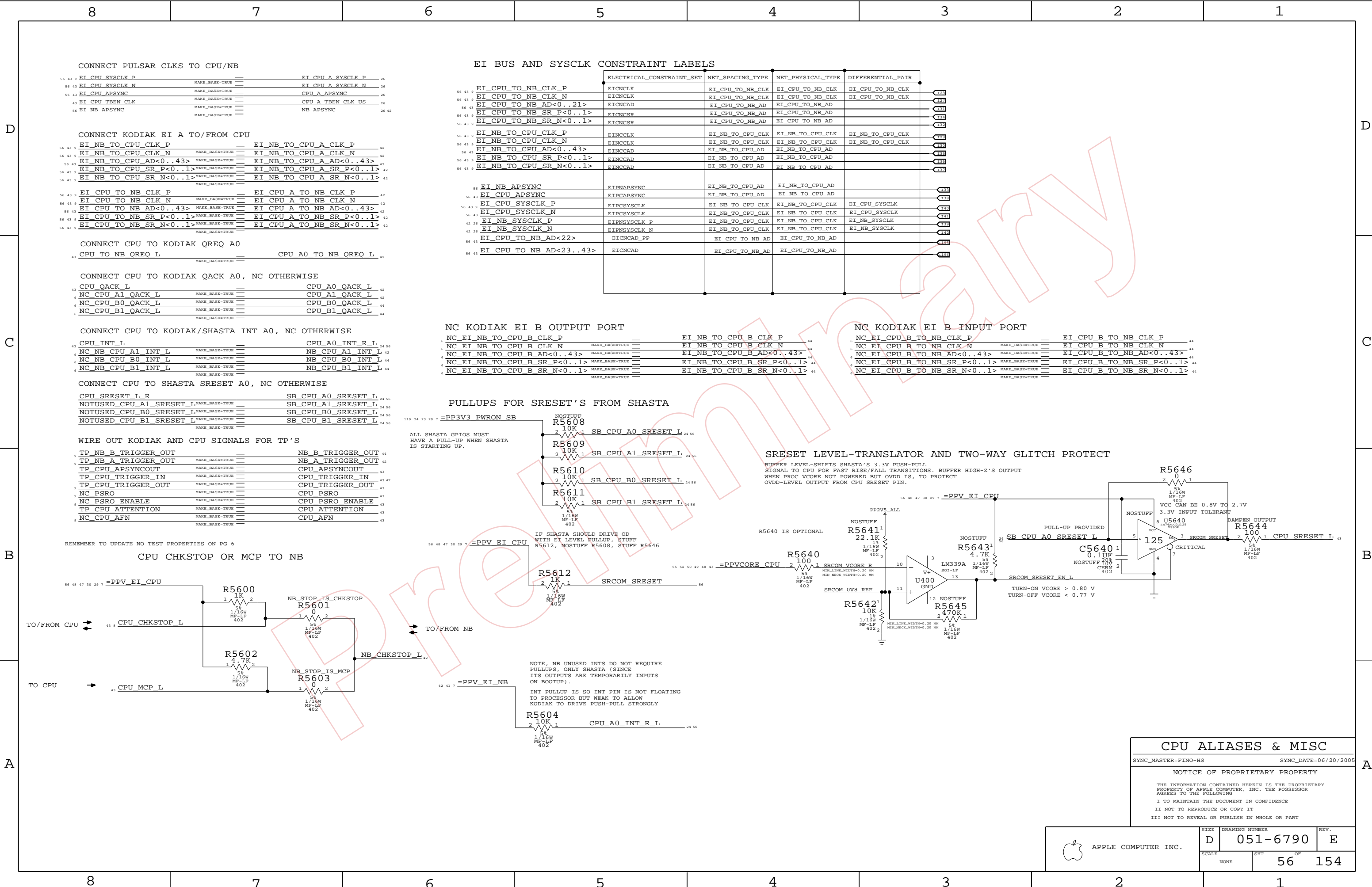
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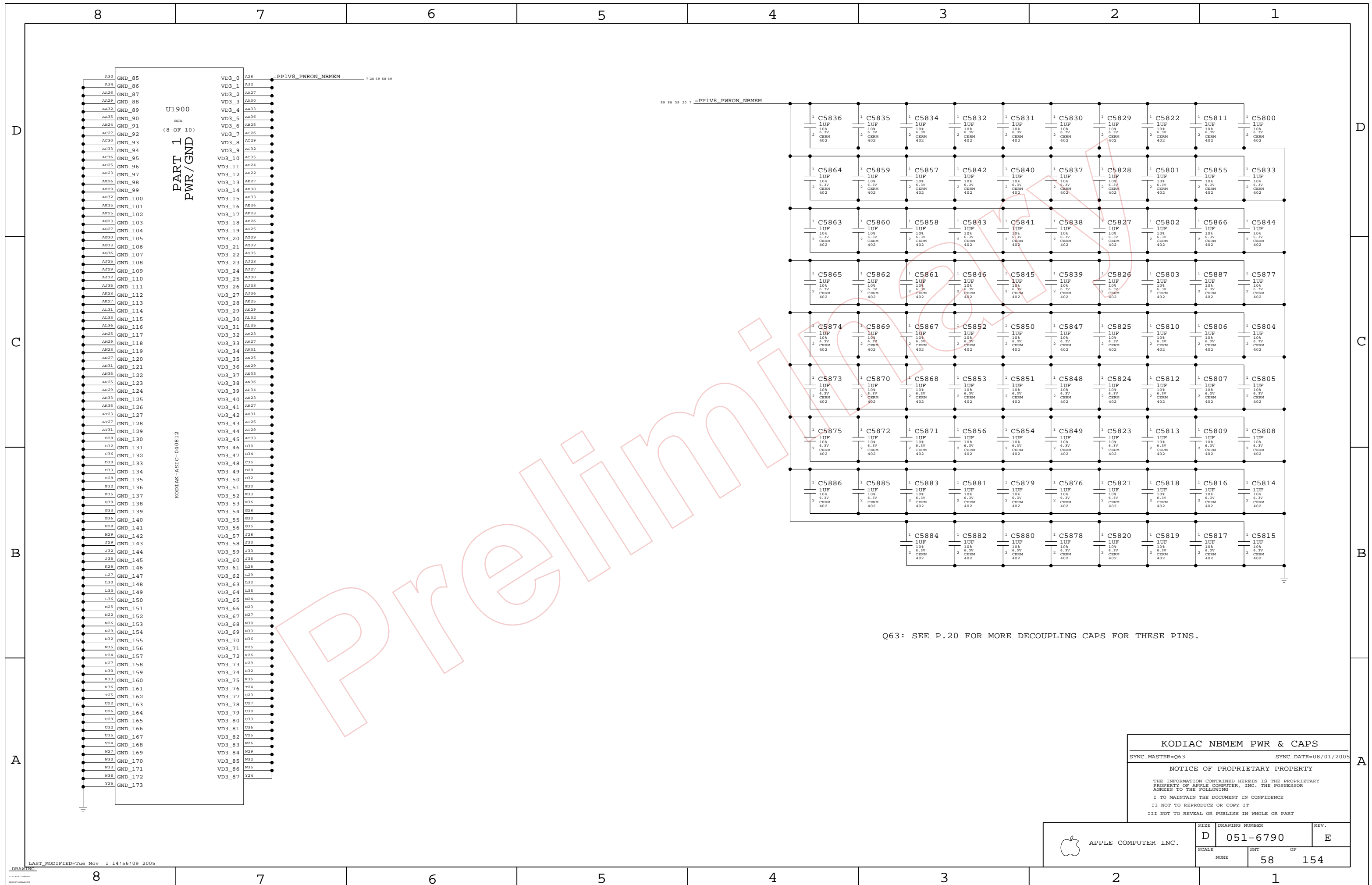
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NONE			





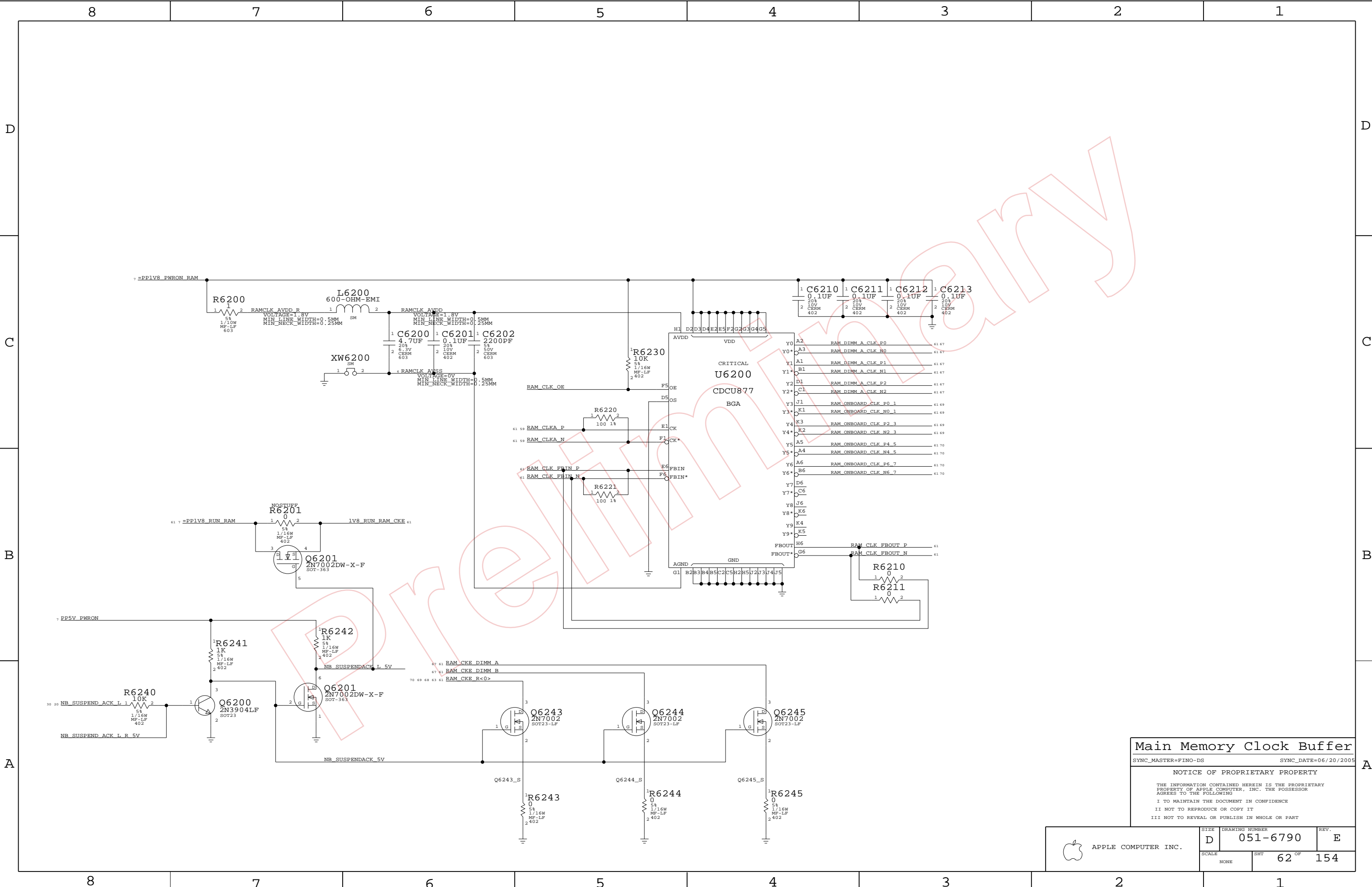












Main Memory Clock Buffer

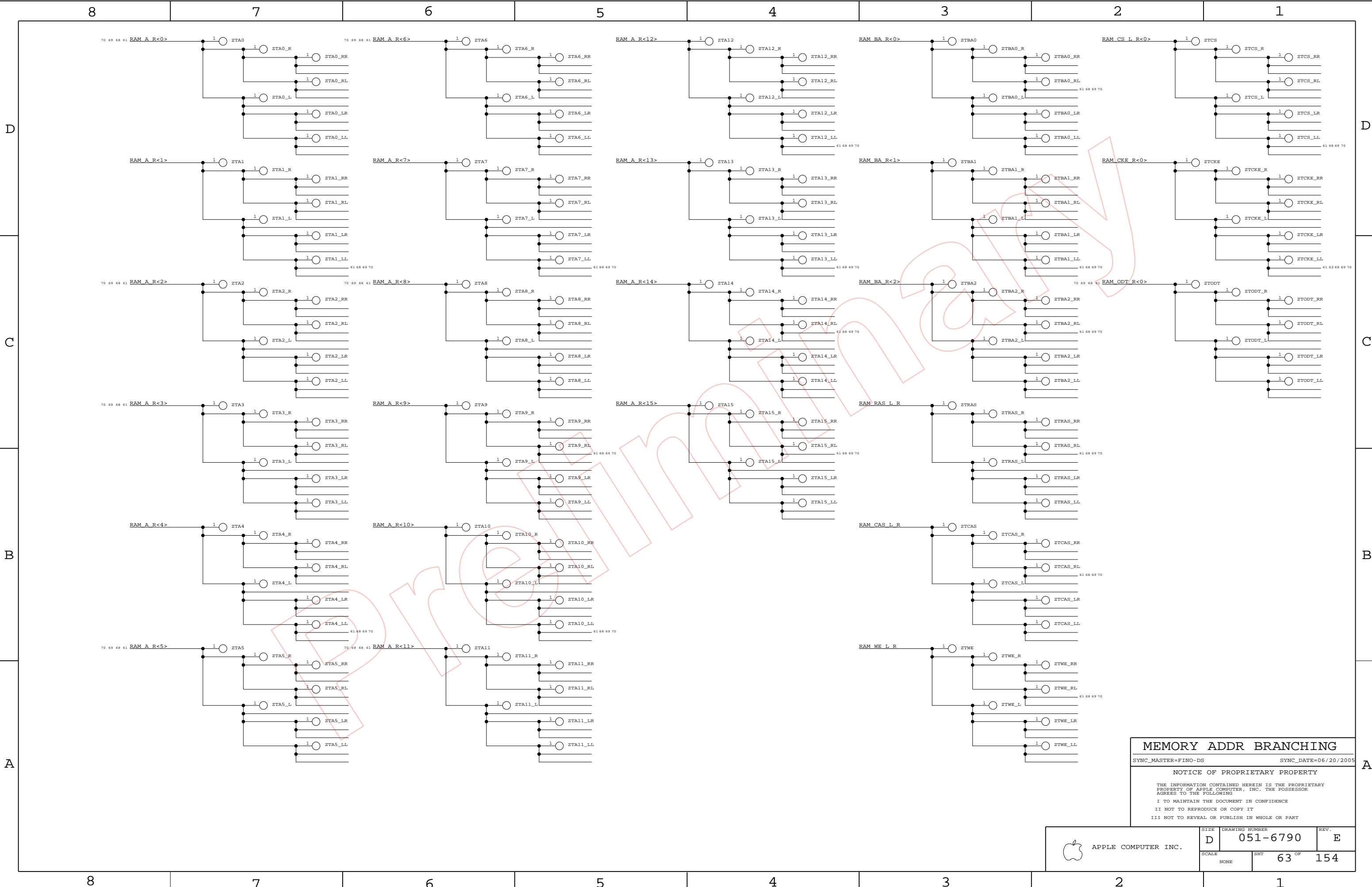
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MEMORY ADDR BRANCHING

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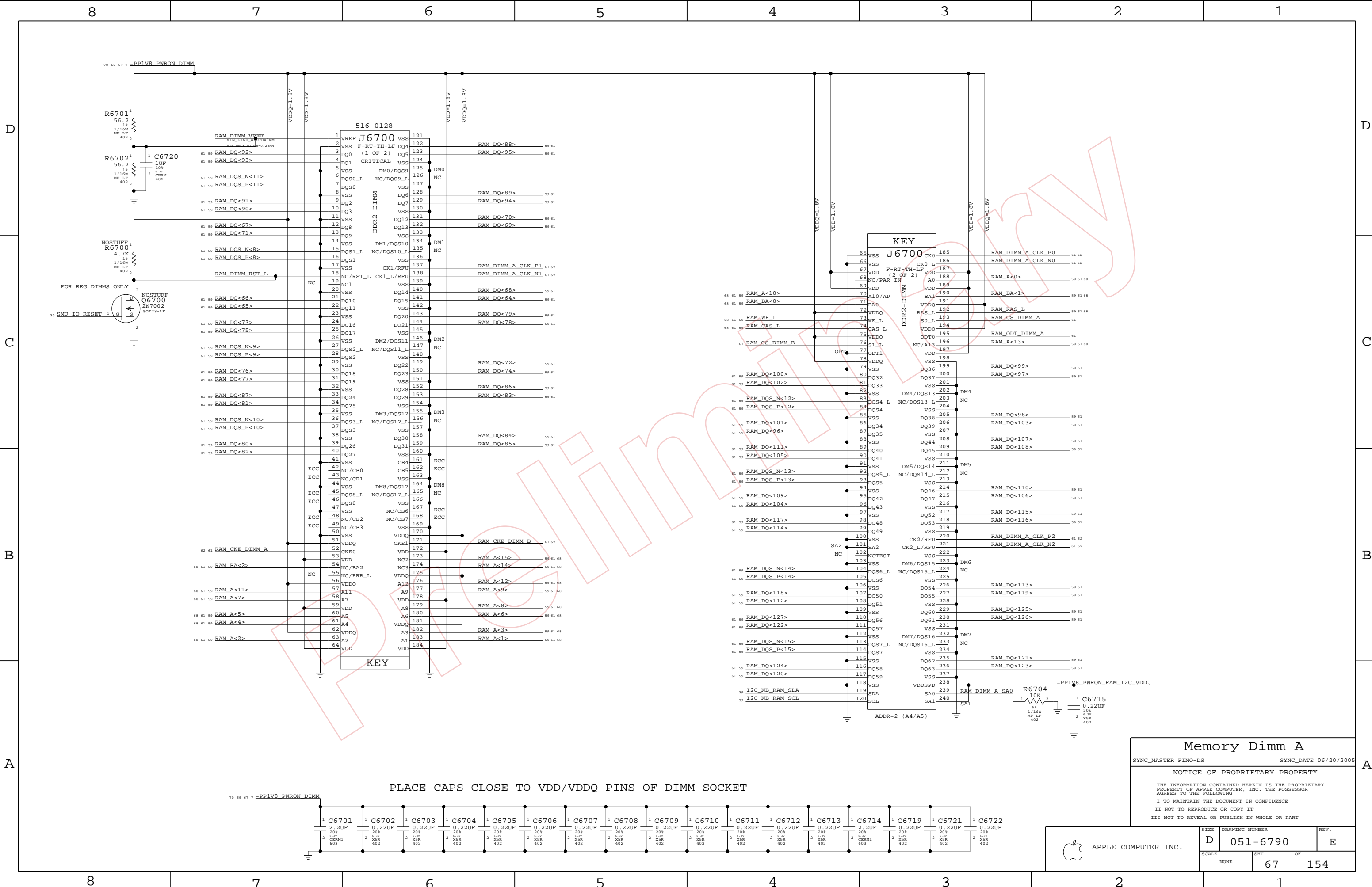
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SCALE		SHT	63 OF 154
NONE			



Memory Dimm A

SYNC\_MASTER=FINO-DS

SYNC\_DATE=06/20/2005

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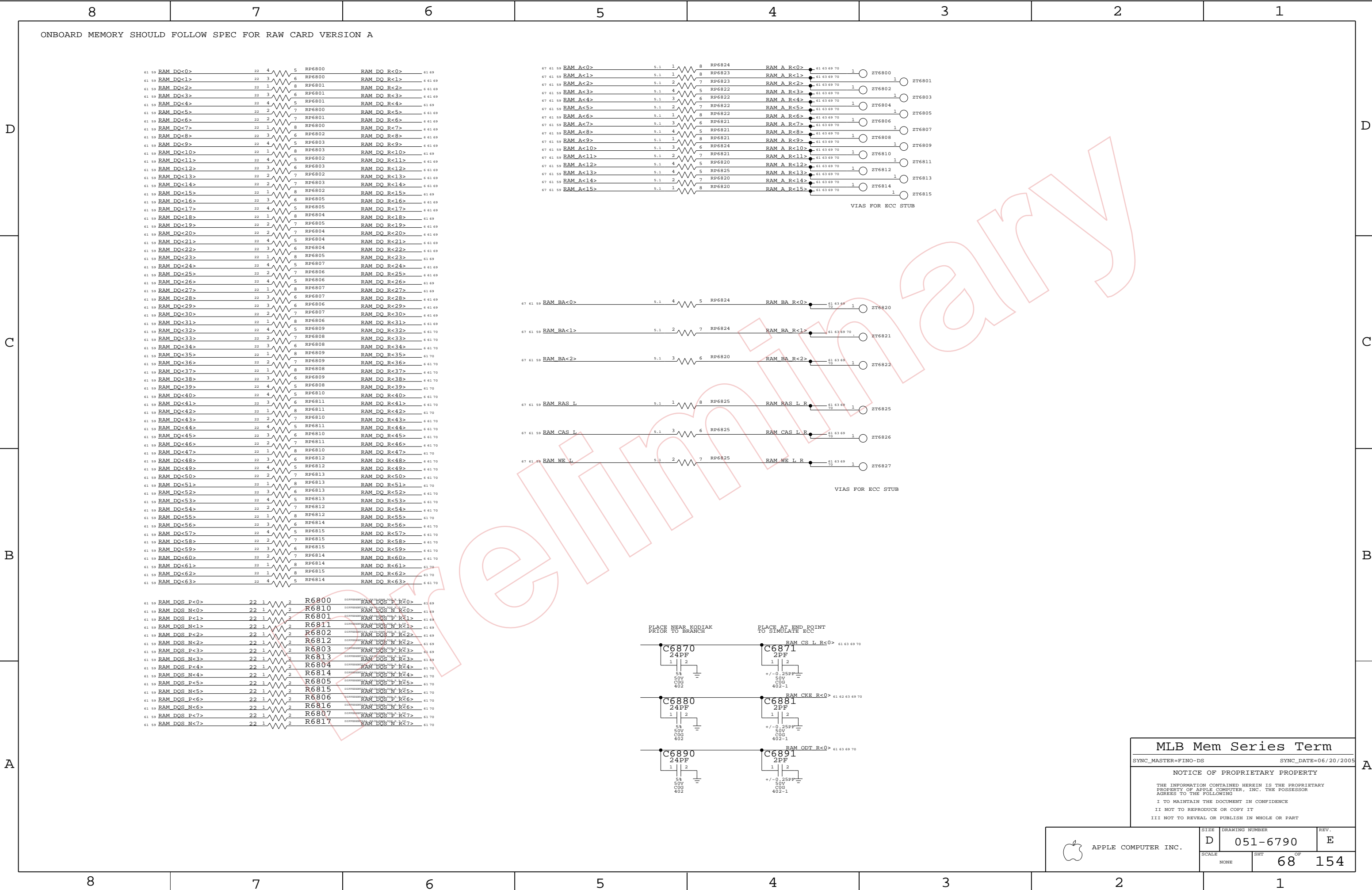
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SCALE		SHT	OF
NONE		67	154



MLB Mem Series Term

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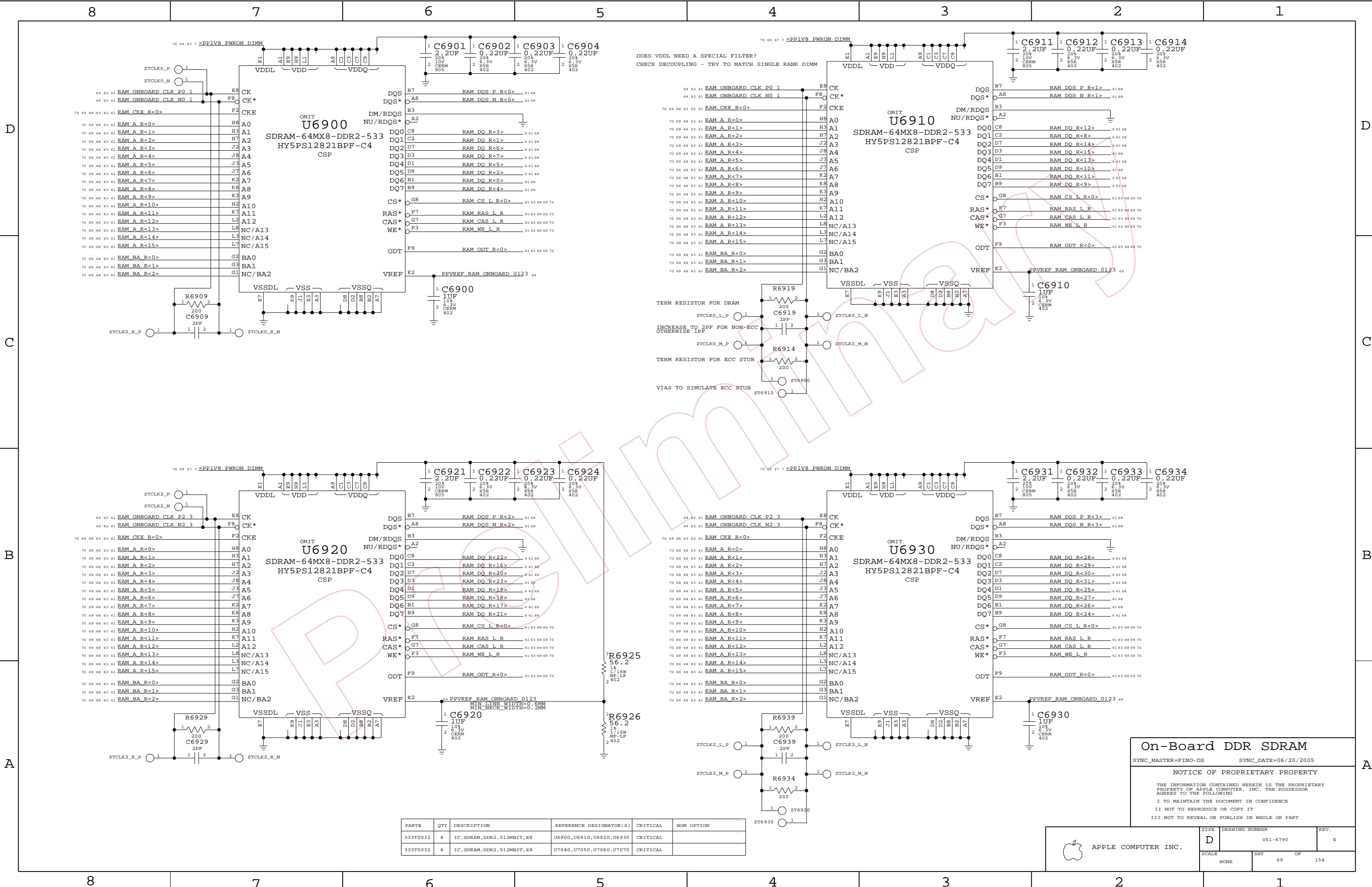
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	D	051-6790	E
SCALE	NONE		SHT
	68		154



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333T0032	4	IC, SDRAM, DDR2, 512MBIT, X8	U6900, U6910, U6920, U6930	CRITICAL	
333T0032	4	IC, SDRAM, DDR2, 512MBIT, X8	U7040, U7050, U7060, U7070	CRITICAL	

On-Board DDR SDRAM

SYNC\_MASTER=FINO-DS      SYNC\_DATE=06/20/2005

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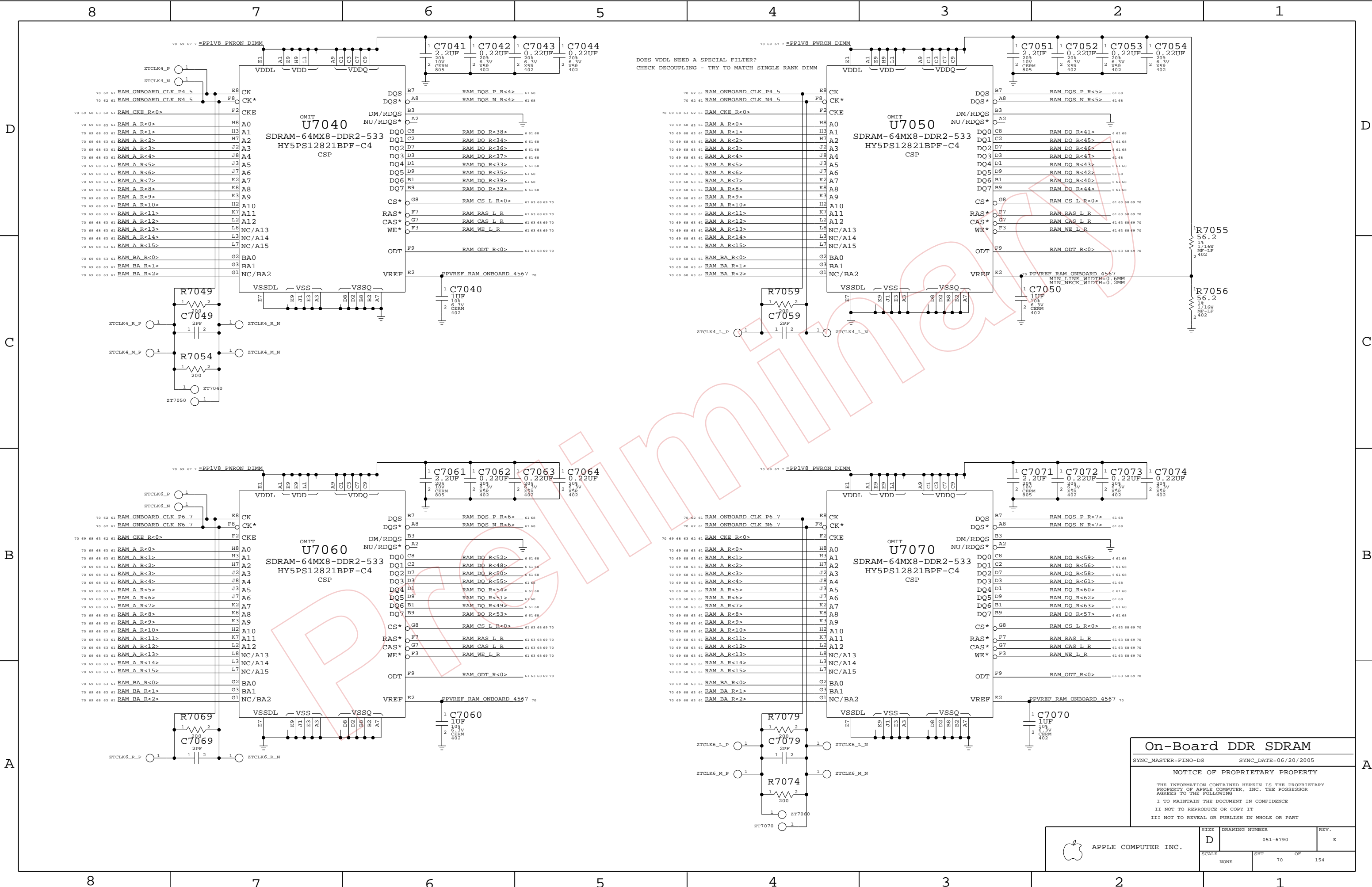


APPLE COMPUTER INC.

SIZE D      DRAWING NUMBER 051-6790      REV. E

SCALE NONE      SHT 69      OF 154





On-Board DDR SDRAM

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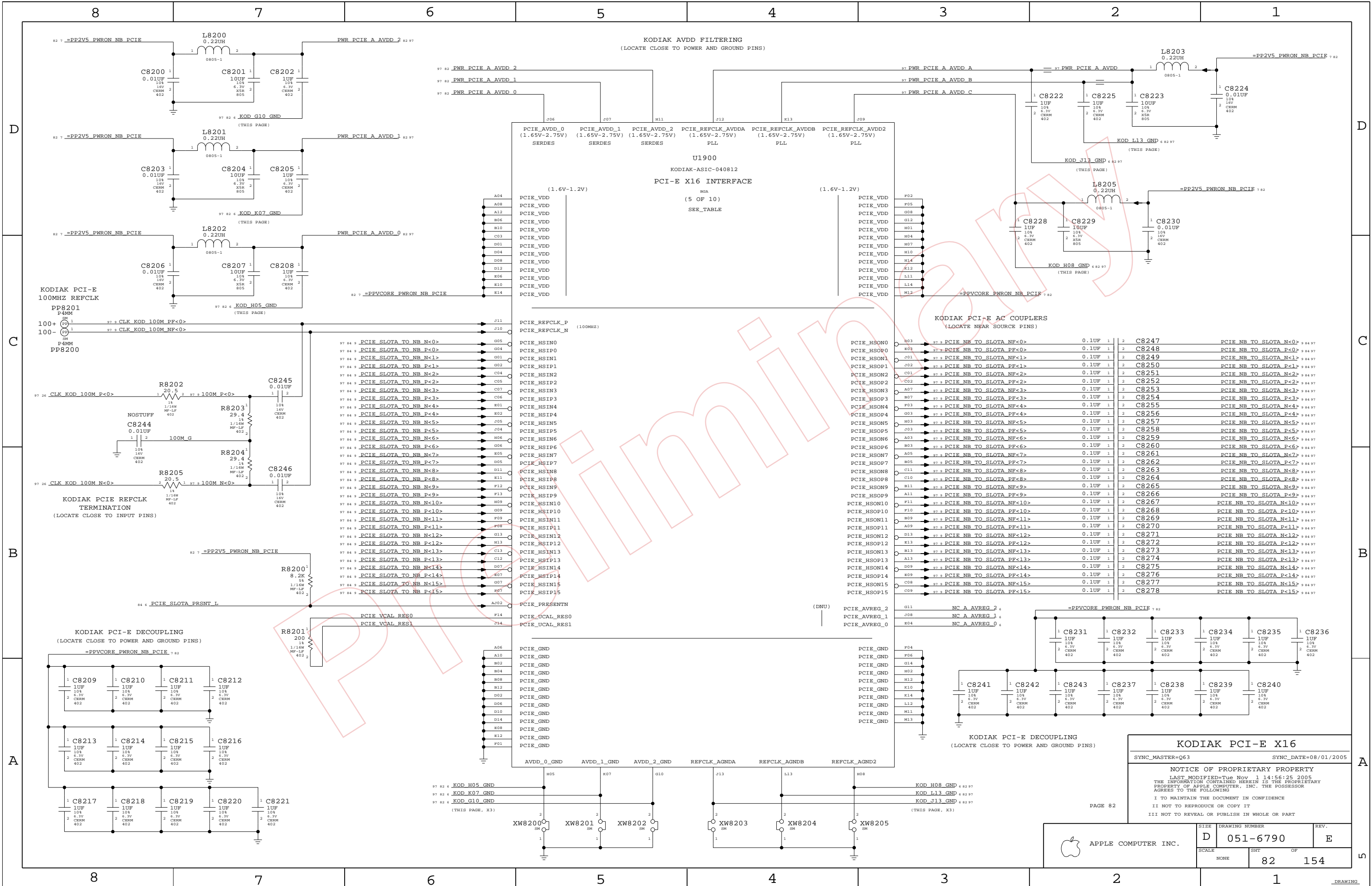
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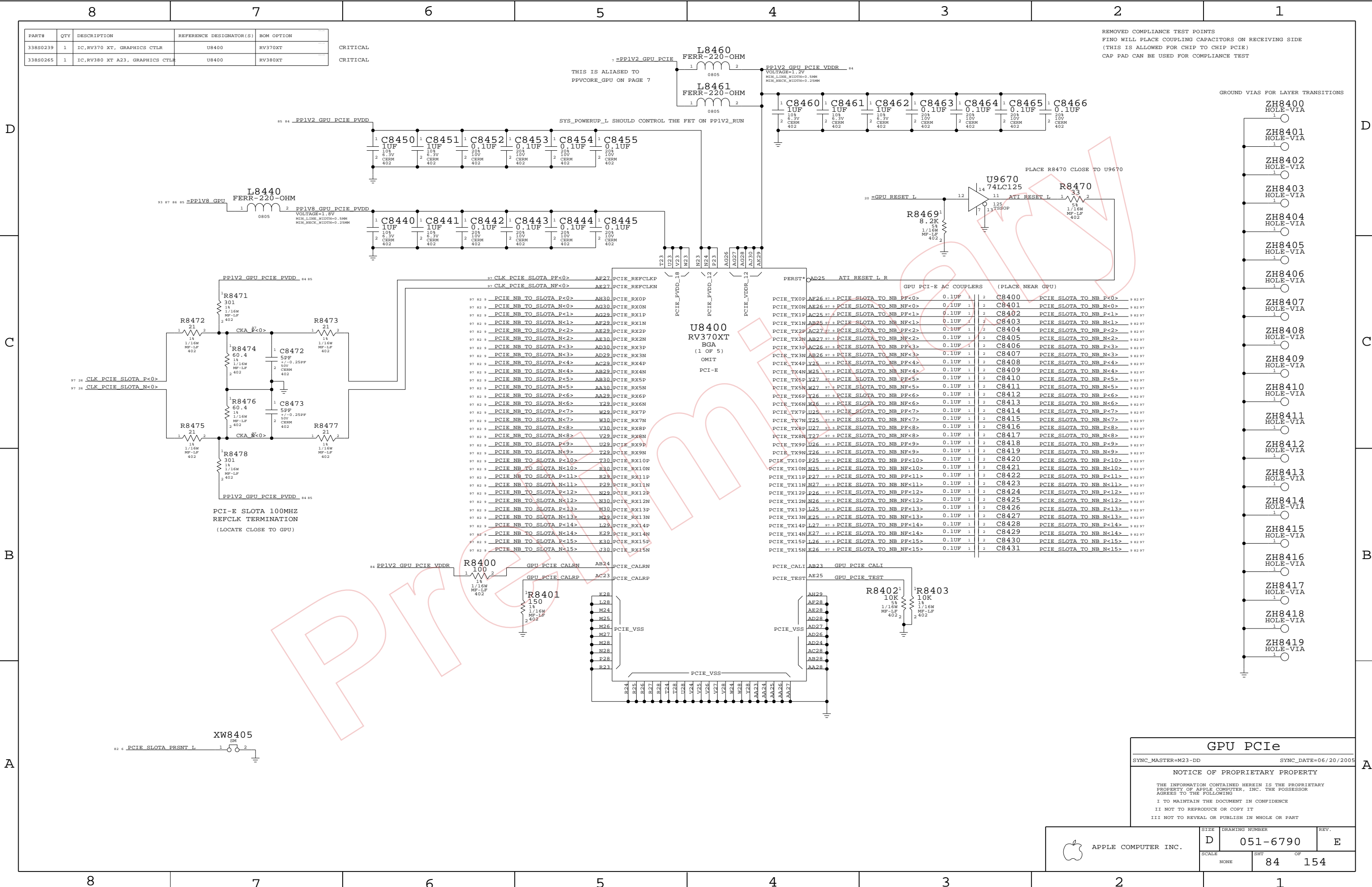
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6790	REV. E
	SCALE NONE	SHT 70	OF 154








PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
338S0239	1	IC,RV370 XT, GRAPHICS CTRL	U8400	RV370XT
338S0265	1	IC,RV380 XT A23, GRAPHICS CTRL	U8400	RV380XT

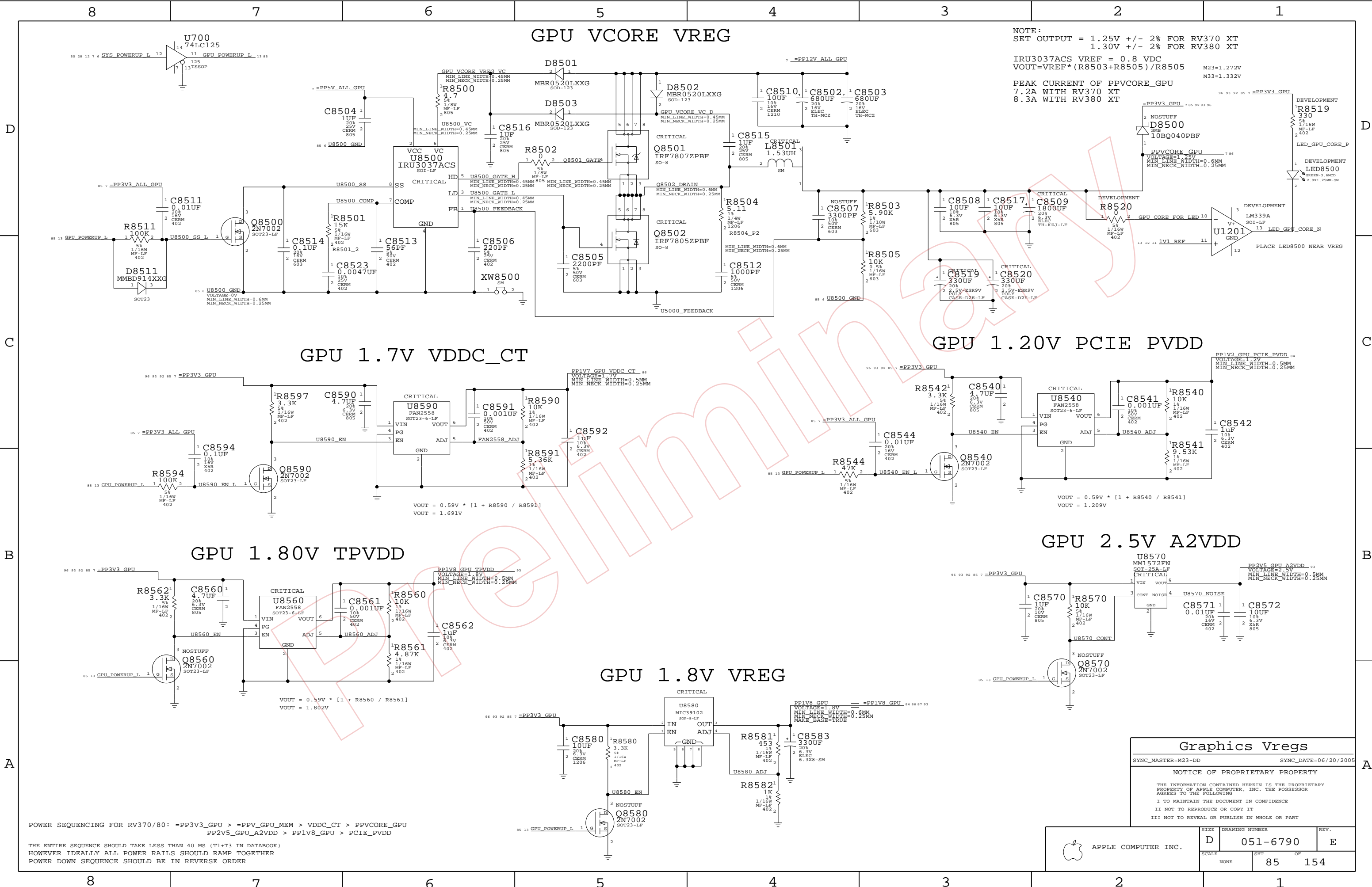
CRITICAL  
CRITICAL

REMOVED COMPLIANCE TEST POINTS  
FINO WILL PLACE COUPLING CAPACITORS ON RECEIVING SIDE  
(THIS IS ALLOWED FOR CHIP TO CHIP PCIe)  
CAP PAD CAN BE USED FOR COMPLIANCE TEST

GROUND VIAS FOR LAYER TRANSITIONS

GPU PCIe	
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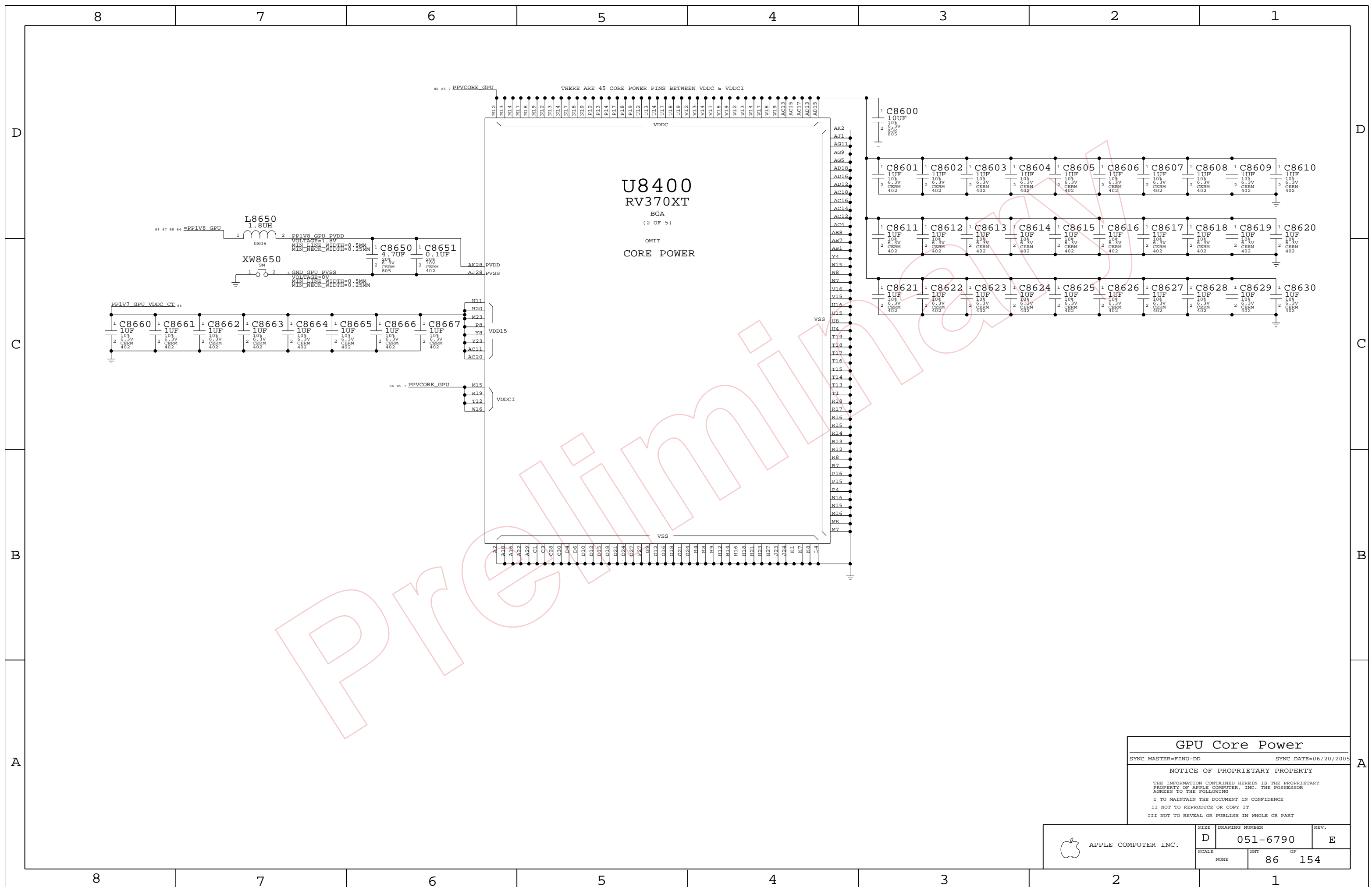
 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6790	REV. E
	SCALE NONE	SHT 84	OF 154



NOTE:  
SET OUTPUT = 1.25V +/- 2% FOR RV370 XT  
1.30V +/- 2% FOR RV380 XT  
IRU3037ACS VREF = 0.8 VDC  
VOUT=VREF\*(R8503+R8505)/R8505  
M23=1.272V  
M33=1.332V  
PEAK CURRENT OF PPVCORE\_GPU  
7.2A WITH RV370 XT  
8.3A WITH RV380 XT

POWER SEQUENCING FOR RV370/80: =PP3V3\_GPU > =PPV\_GPU\_MEM > VDDC\_CT > PPVCORE\_GPU  
PP2V5\_GPU\_A2VDD > PP1V8\_GPU > PCIE\_PVDD  
THE ENTIRE SEQUENCE SHOULD TAKE LESS THAN 40 MS (T1+T3 IN DATABOOK)  
HOWEVER IDEALLY ALL POWER RAILS SHOULD RAMP TOGETHER  
POWER DOWN SEQUENCE SHOULD BE IN REVERSE ORDER

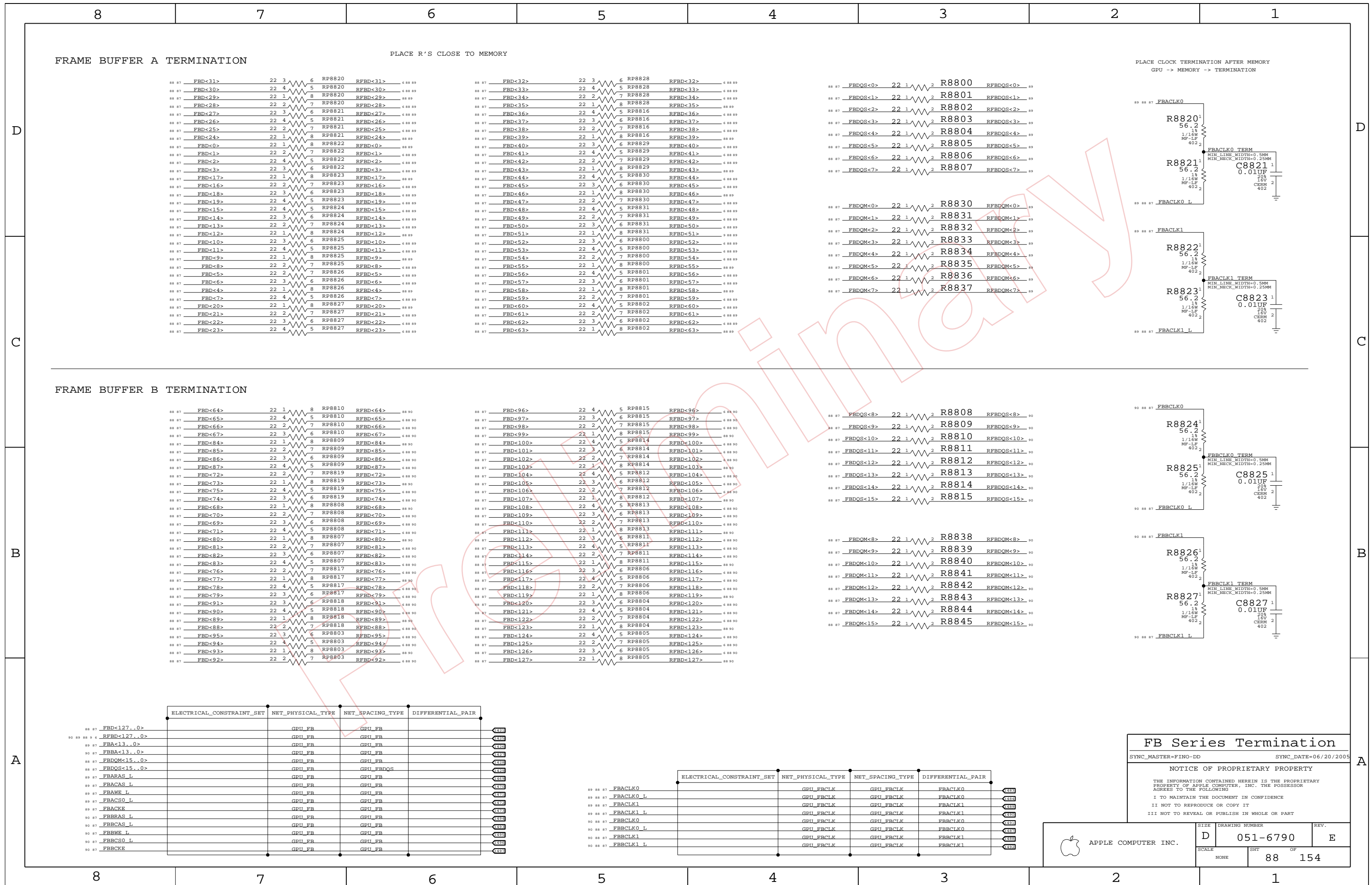
Graphics Vregs			
SYNC_MASTER=M23-DD		SYNC_DATE=06/20/2005	
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COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
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	SCALE	SHT	OF
	NONE	85	154

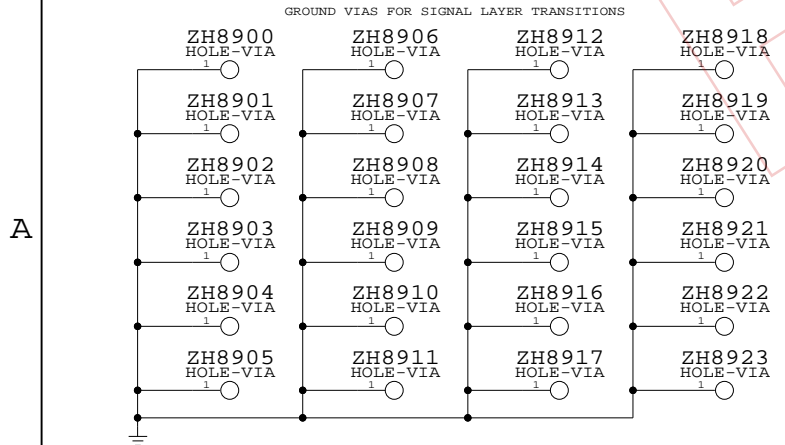
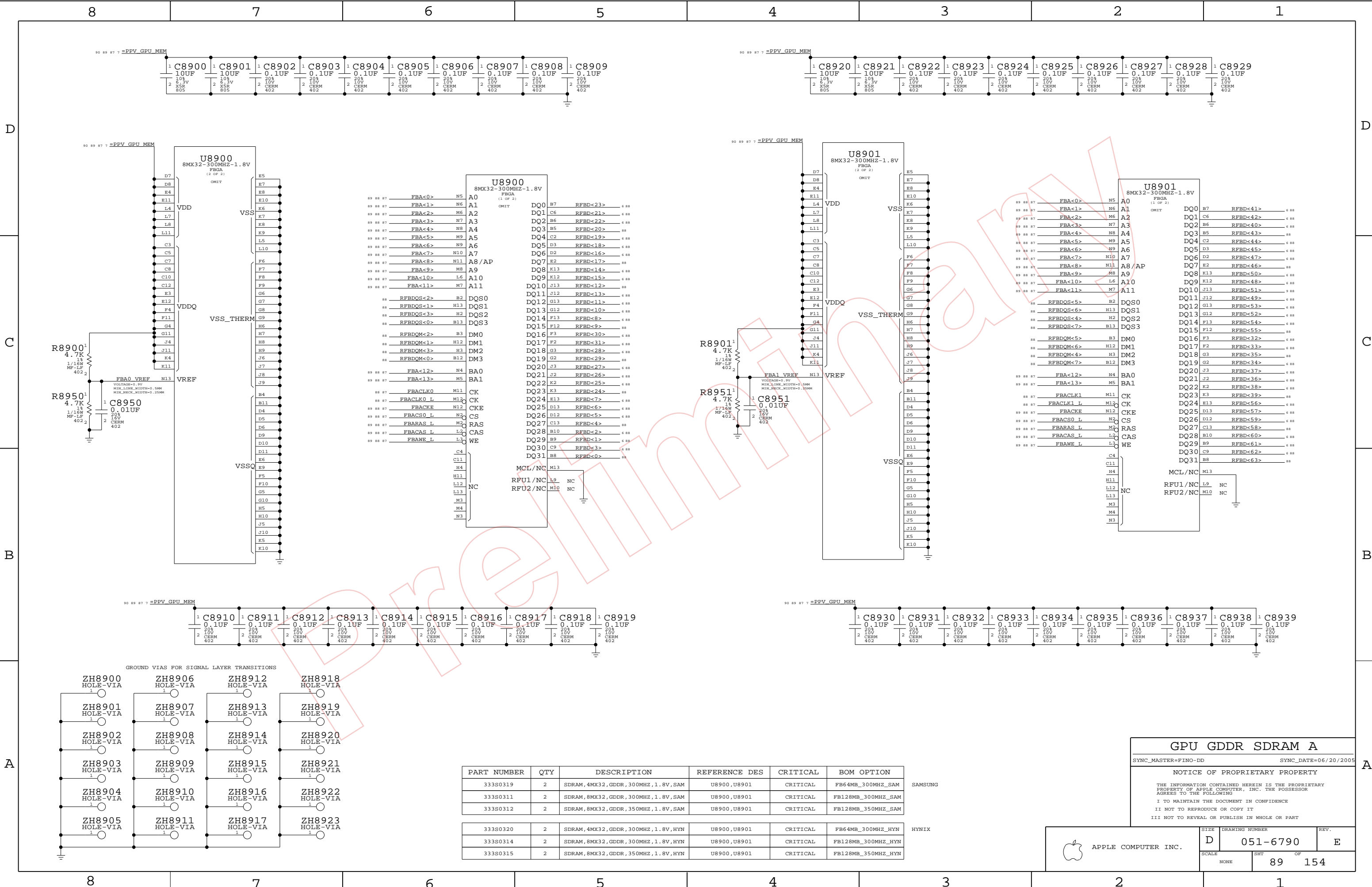












PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0319	2	SDRAM, 4MX32, GDDR, 300MHZ, 1.8V, SAM	U8900, U8901	CRITICAL	FB64MB_300MHZ_SAM
333S0311	2	SDRAM, 8MX32, GDDR, 300MHZ, 1.8V, SAM	U8900, U8901	CRITICAL	FB128MB_300MHZ_SAM
333S0312	2	SDRAM, 8MX32, GDDR, 350MHZ, 1.8V, SAM	U8900, U8901	CRITICAL	FB128MB_350MHZ_SAM
333S0320	2	SDRAM, 4MX32, GDDR, 300MHZ, 1.8V, HYN	U8900, U8901	CRITICAL	FB64MB_300MHZ_HYN
333S0314	2	SDRAM, 8MX32, GDDR, 300MHZ, 1.8V, HYN	U8900, U8901	CRITICAL	FB128MB_300MHZ_HYN
333S0315	2	SDRAM, 8MX32, GDDR, 350MHZ, 1.8V, HYN	U8900, U8901	CRITICAL	FB128MB_350MHZ_HYN

GPU GDDR SDRAM A

SYNC\_MASTER=FINO-DD

SYNC\_DATE=06/20/2005

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D051-6790E

SCALE: NONE

SHT: 89

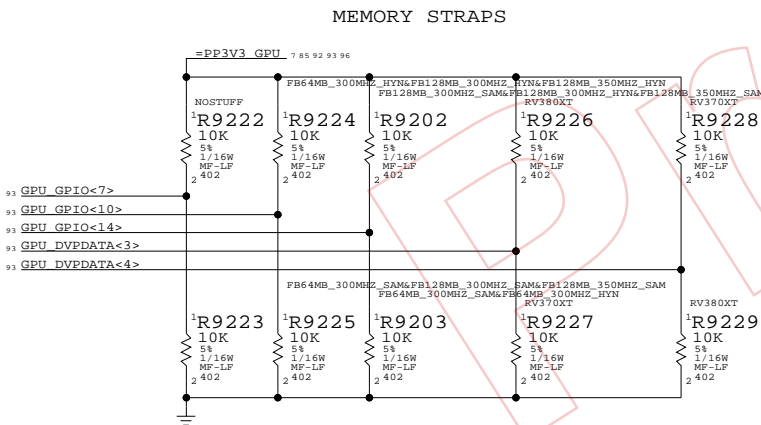
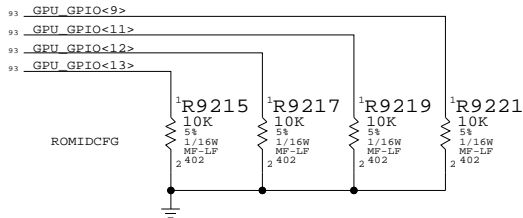
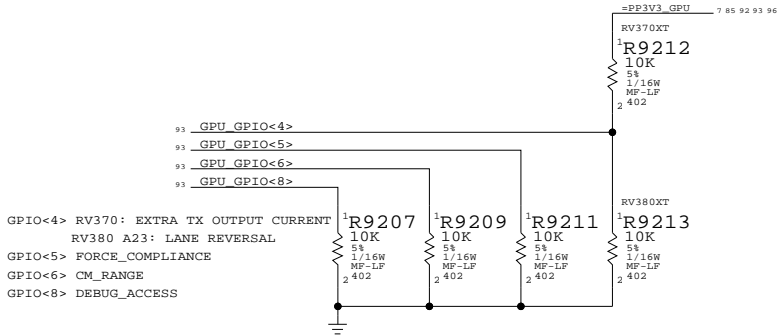
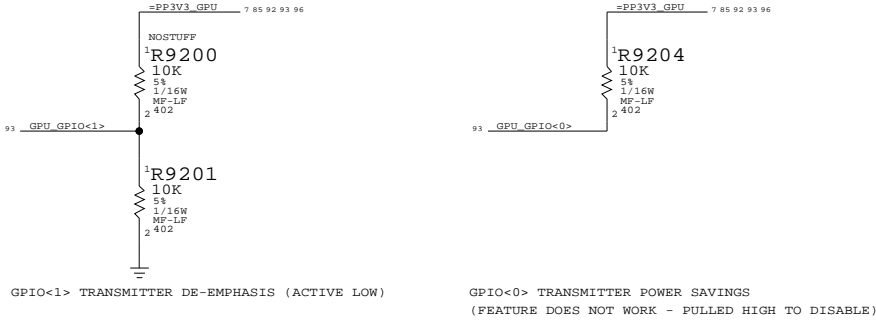
OF: 154

REV: E

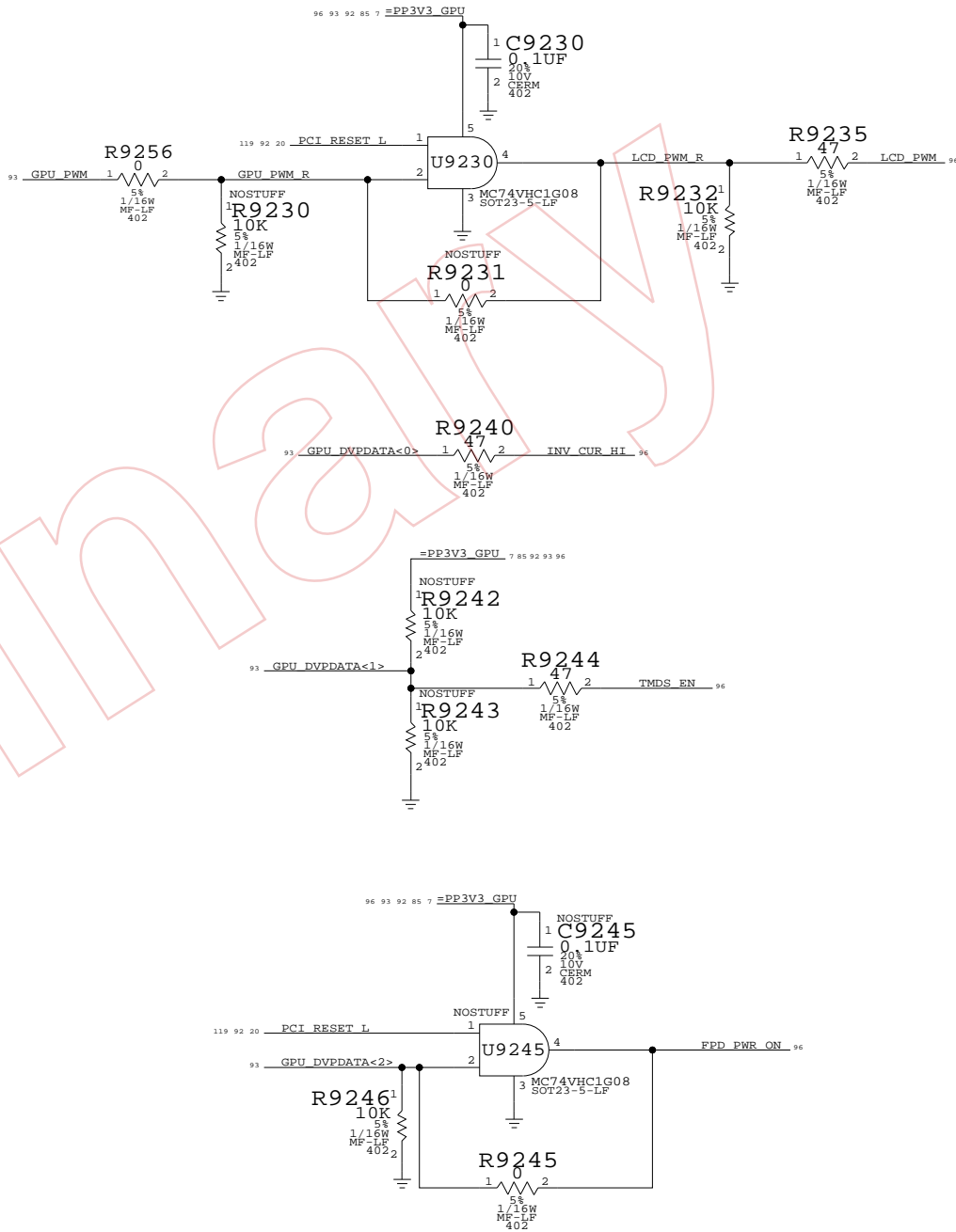


ATI STRAPS

APPLE GPIOS



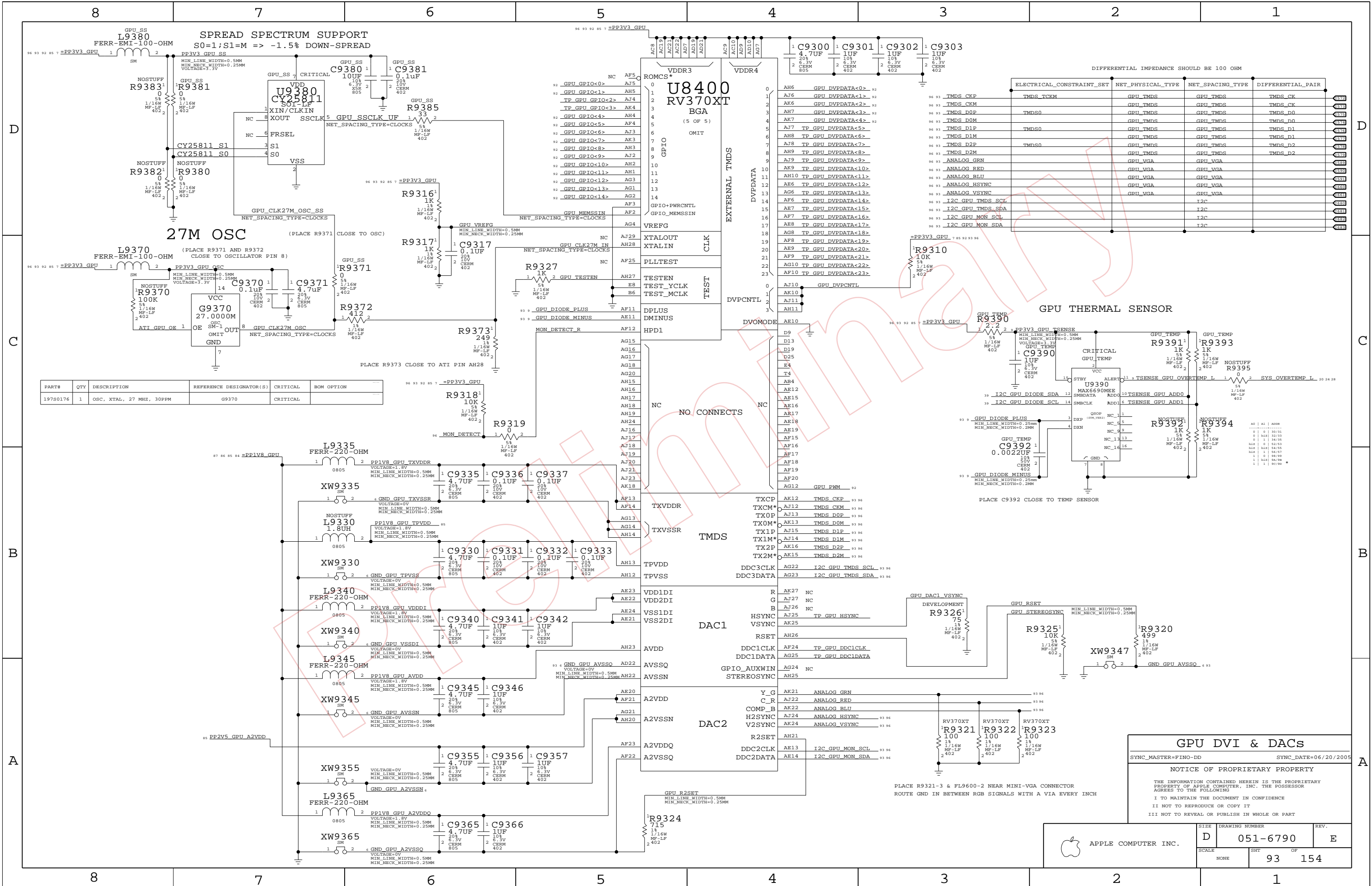
GPIO<7> - MEMORY DIE REVISION  
0 - ORIGINAL DIE REVISION  
1 - NEW (FUTURE) DIE REV  
GPIO<10> - MEMORY VENDOR  
0 - SAMSUNG  
1 - HYNIX  
GPIO<14> - MEMORY DENSITY  
0 - 4MX32  
1 - 8MX32  
DVDPDATA<3,4> - SPEED  
00 - 325E / 200M  
01 - 400E / 300M  
10 - 500E / 350M  
11 - RESERVED FOR FUTURE USE



GPU Straps		
SYNC_MASTER=FINO-DD		SYNC_DATE=06/20/2005
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	E
SCALE		SHT	OF
NONE		92	154





PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0176	1	OSC, XTAL, 27 MHZ, 30PPM	G9370	CRITICAL	

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
TMDS CKP	GPU_TMDS	GPU_TMDS	TMDS_CK
TMDS CKM	GPU_TMDS	GPU_TMDS	TMDS_CK
TMDS D0P	GPU_TMDS	GPU_TMDS	TMDS_D0
TMDS D0M	GPU_TMDS	GPU_TMDS	TMDS_D0
TMDS D1P	GPU_TMDS	GPU_TMDS	TMDS_D1
TMDS D1M	GPU_TMDS	GPU_TMDS	TMDS_D1
TMDS D2P	GPU_TMDS	GPU_TMDS	TMDS_D2
TMDS D2M	GPU_TMDS	GPU_TMDS	TMDS_D2
ANALOG GRN	GPU_VGA	GPU_VGA	GPU_VGA
ANALOG RED	GPU_VGA	GPU_VGA	GPU_VGA
ANALOG BLU	GPU_VGA	GPU_VGA	GPU_VGA
ANALOG HSYNC	GPU_VGA	GPU_VGA	GPU_VGA
ANALOG VSYNC	GPU_VGA	GPU_VGA	GPU_VGA
I2C GPU TMDS_SCL	T2C	T2C	T2C
I2C GPU TMDS_SDA	T2C	T2C	T2C
I2C GPU MON_SCL	T2C	T2C	T2C
I2C GPU MON_SDA	T2C	T2C	T2C

GPU DVI & DACs

SYNC\_MASTER=FINO-DD SYNC\_DATE=06/20/2005

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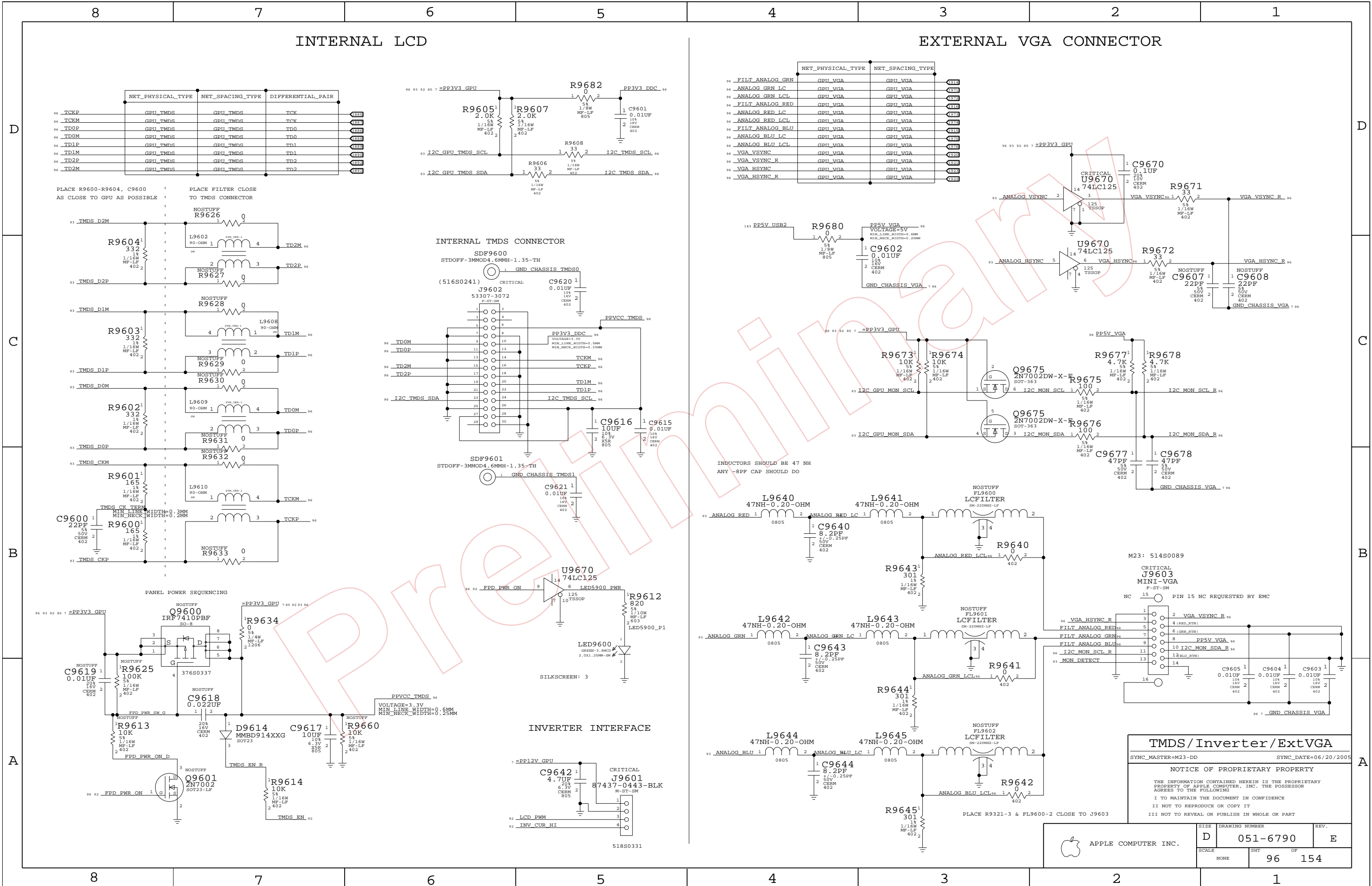
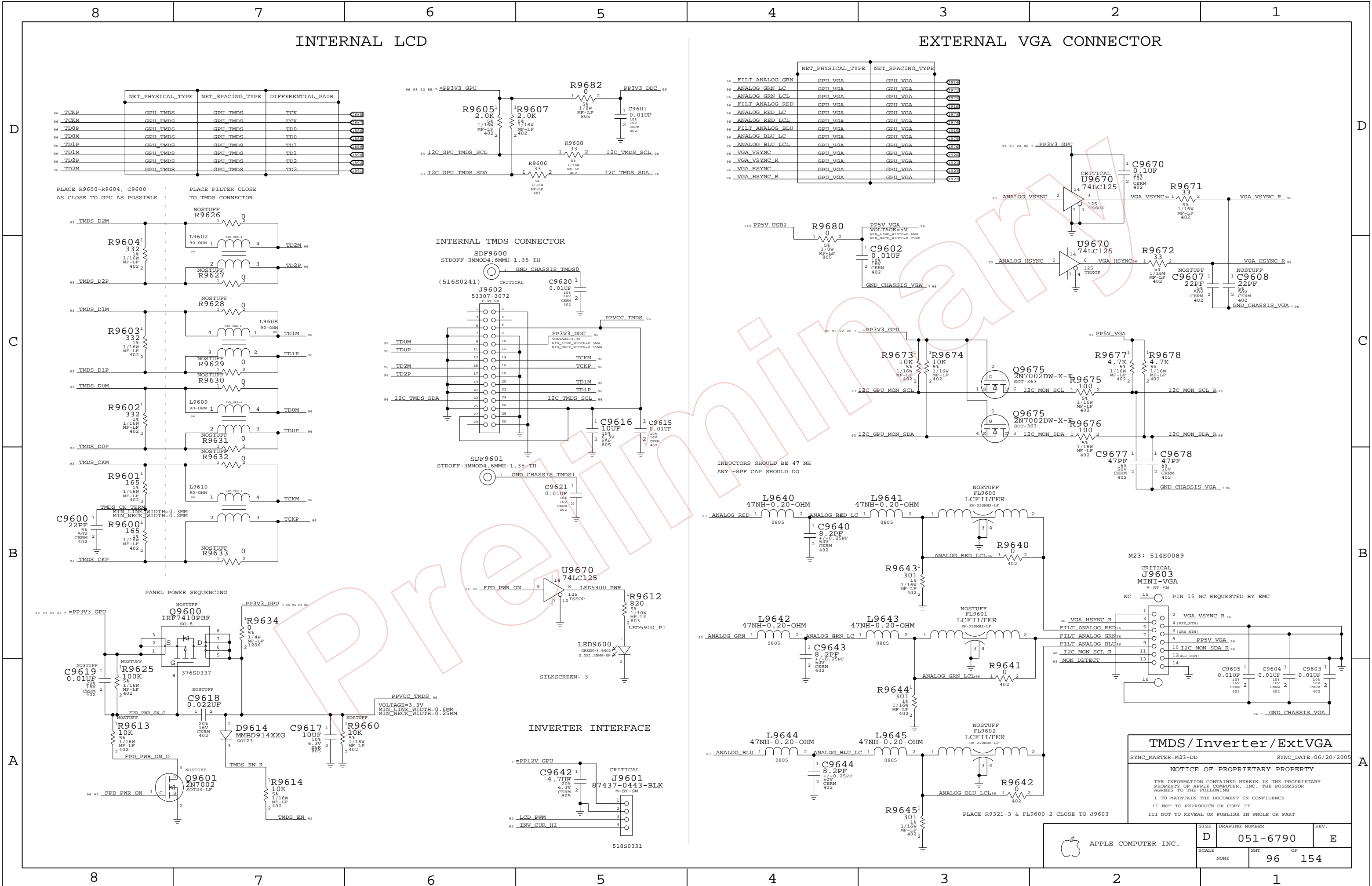
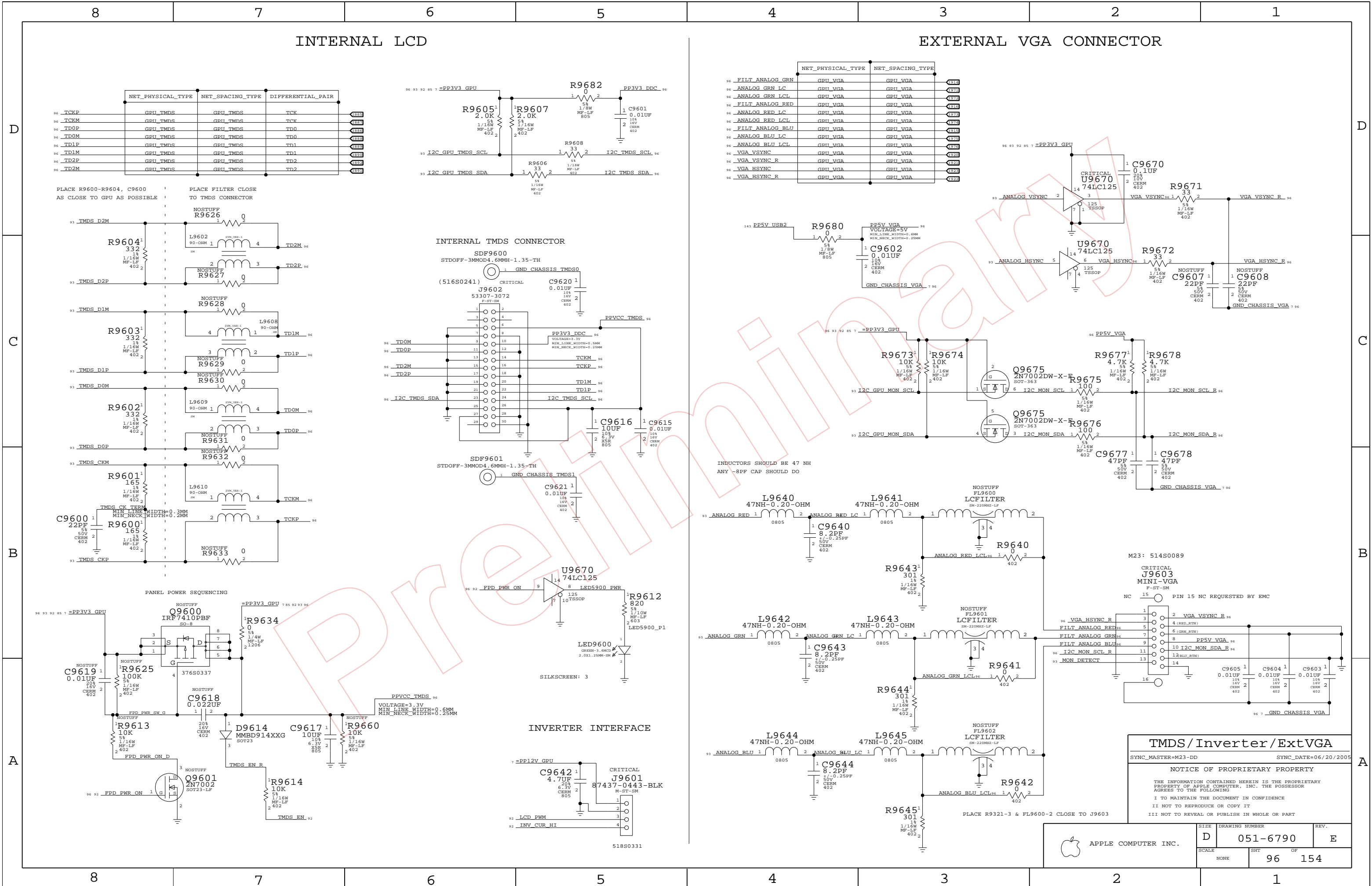
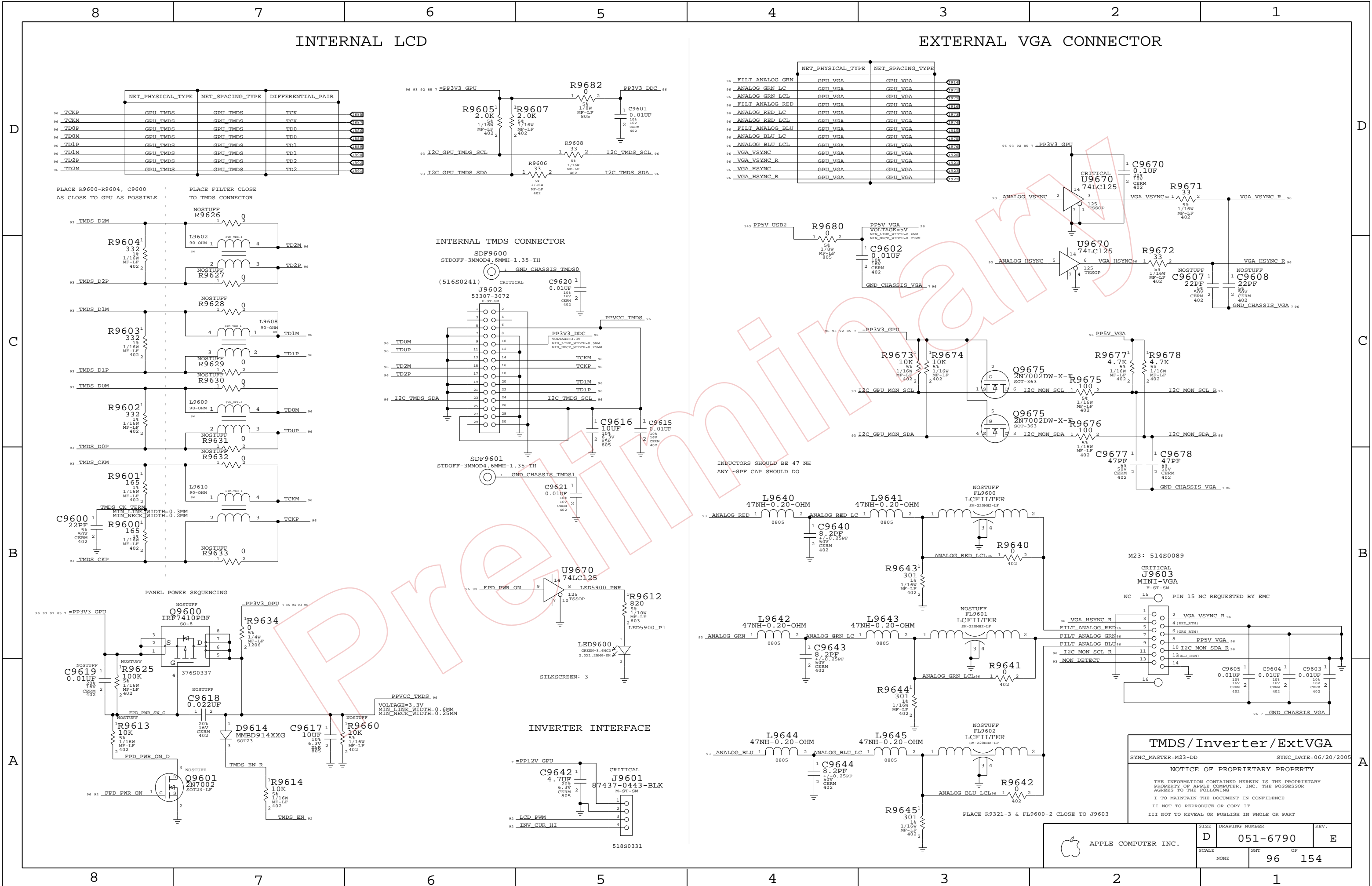
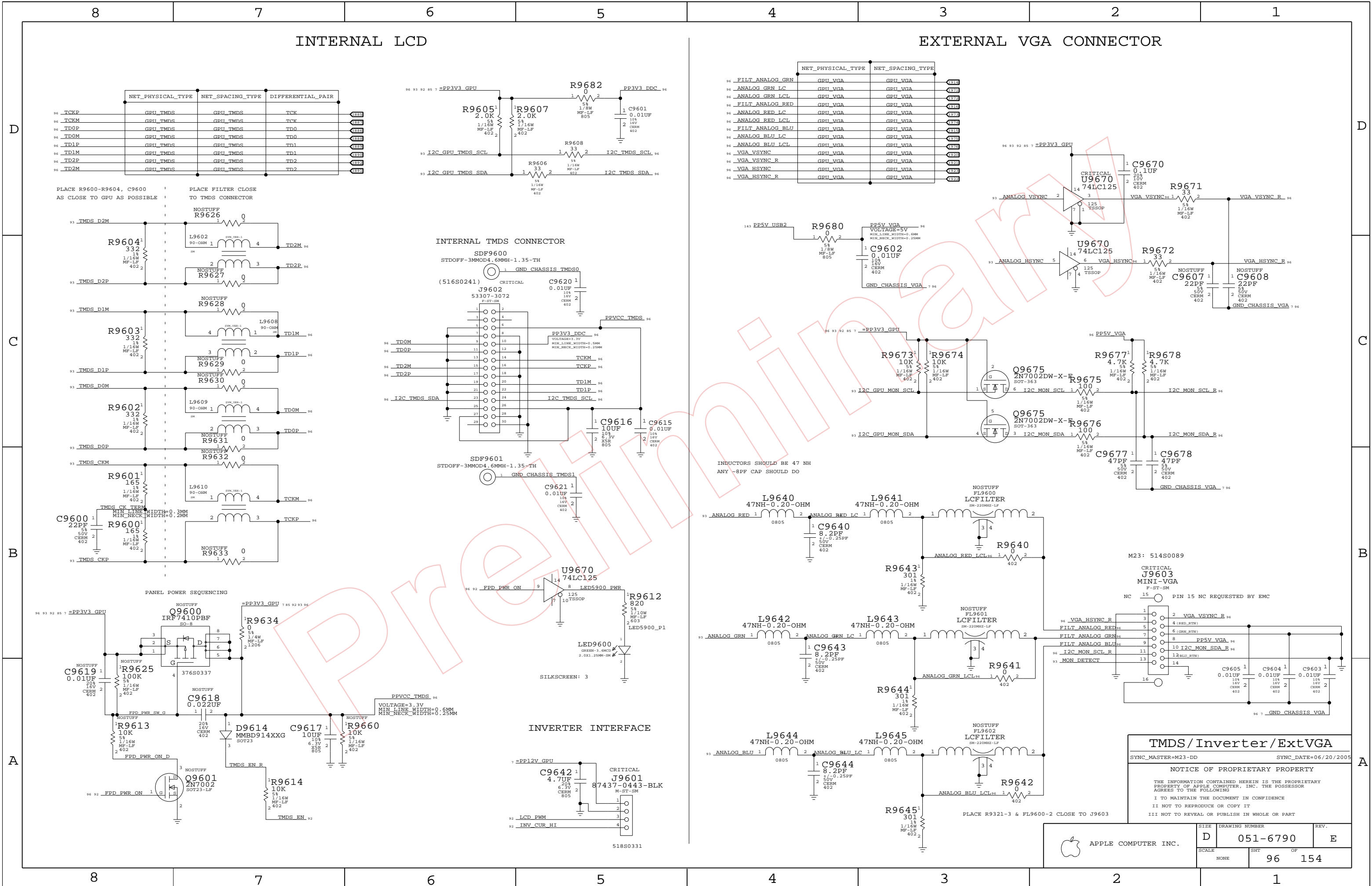
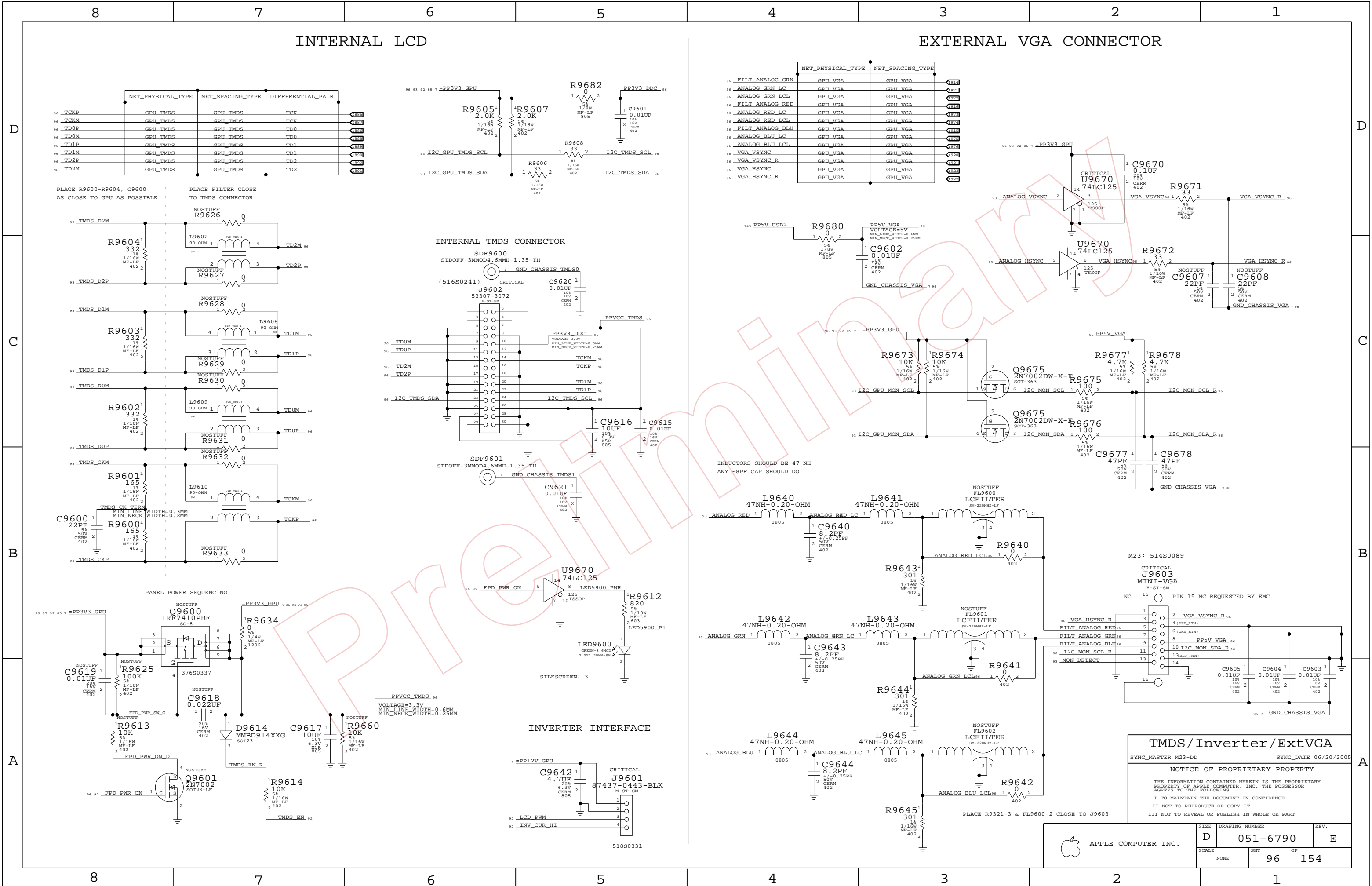
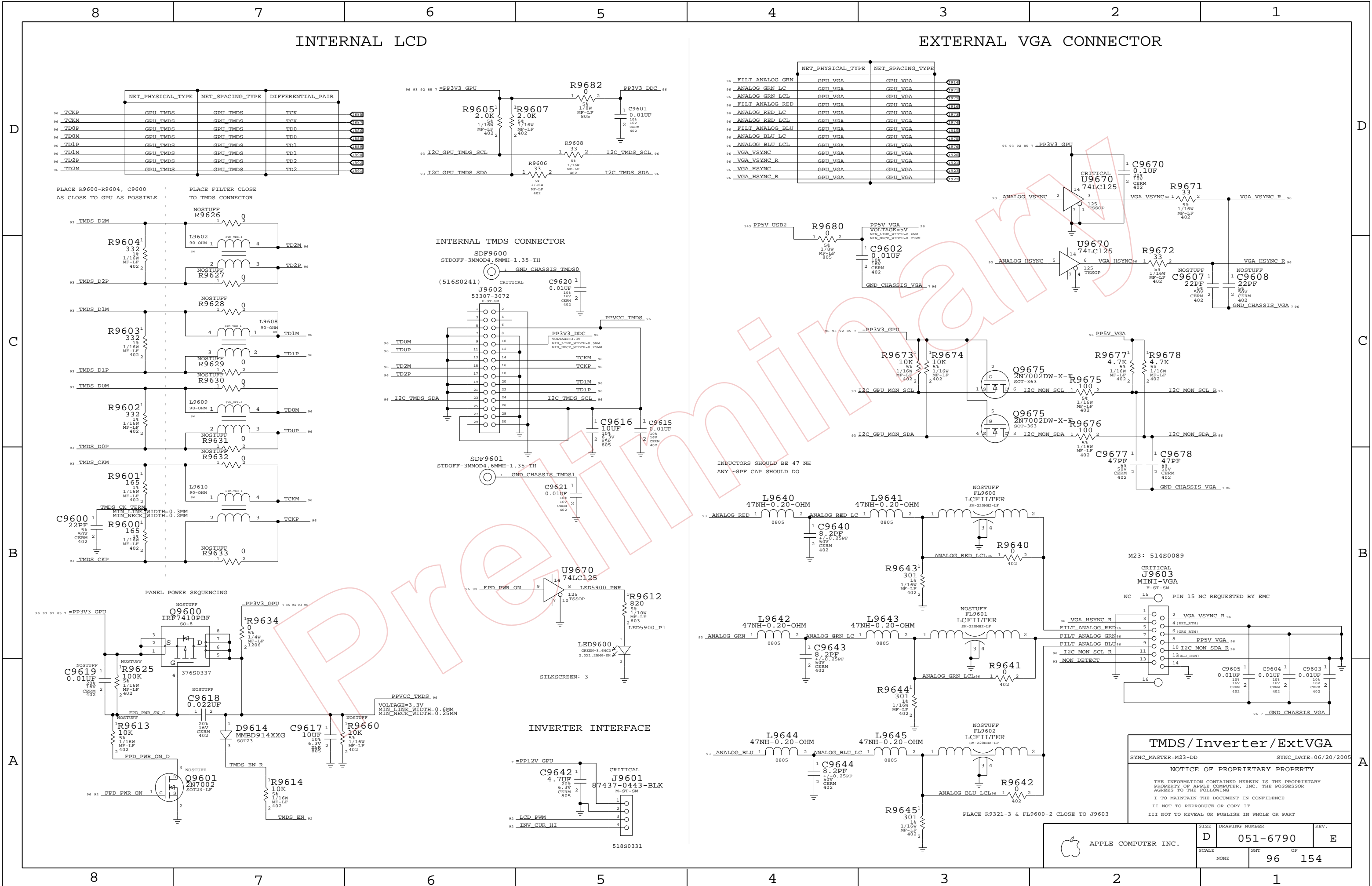
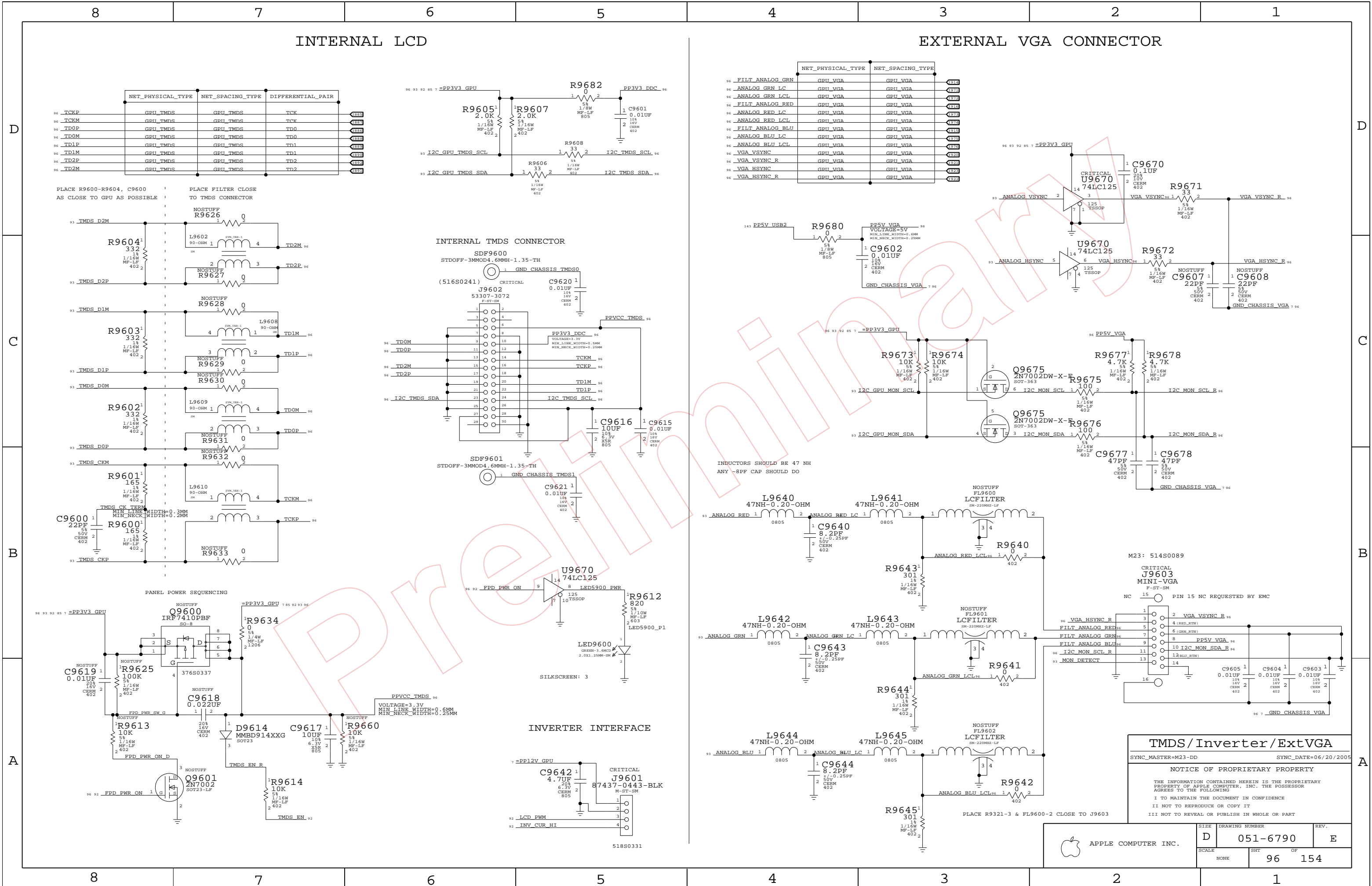
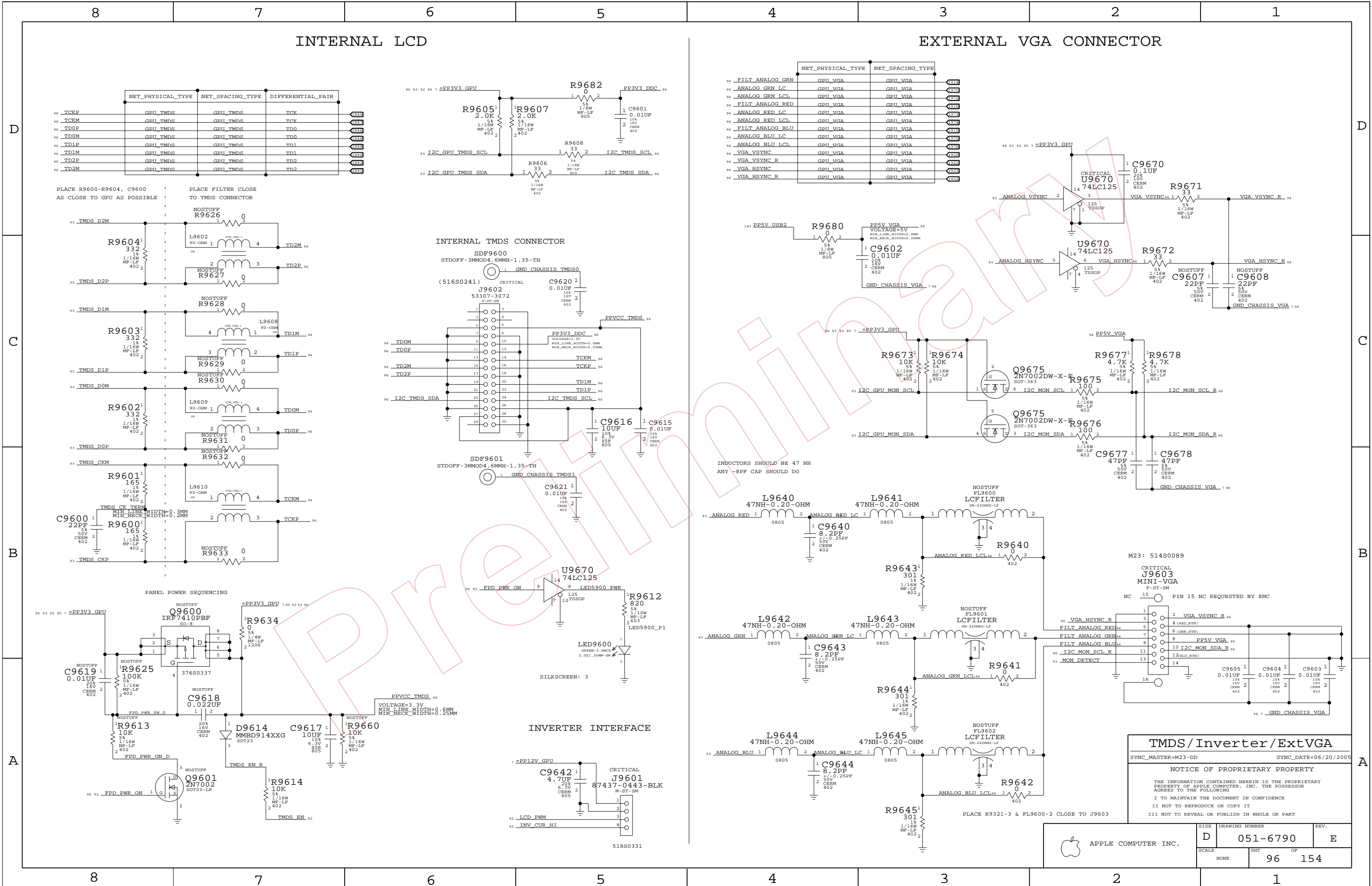
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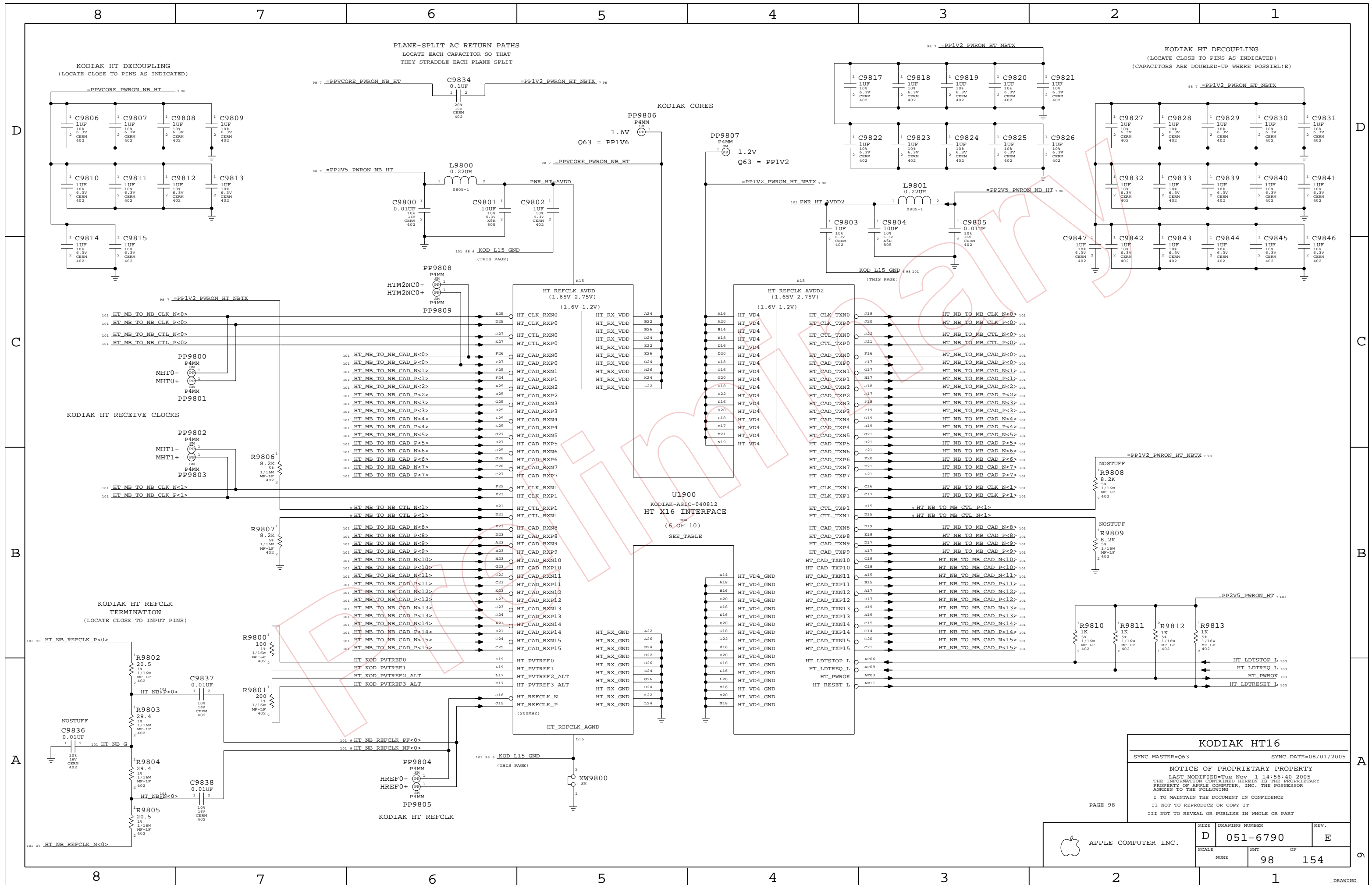
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	SCALE	NONE	SHT	93	OF	154








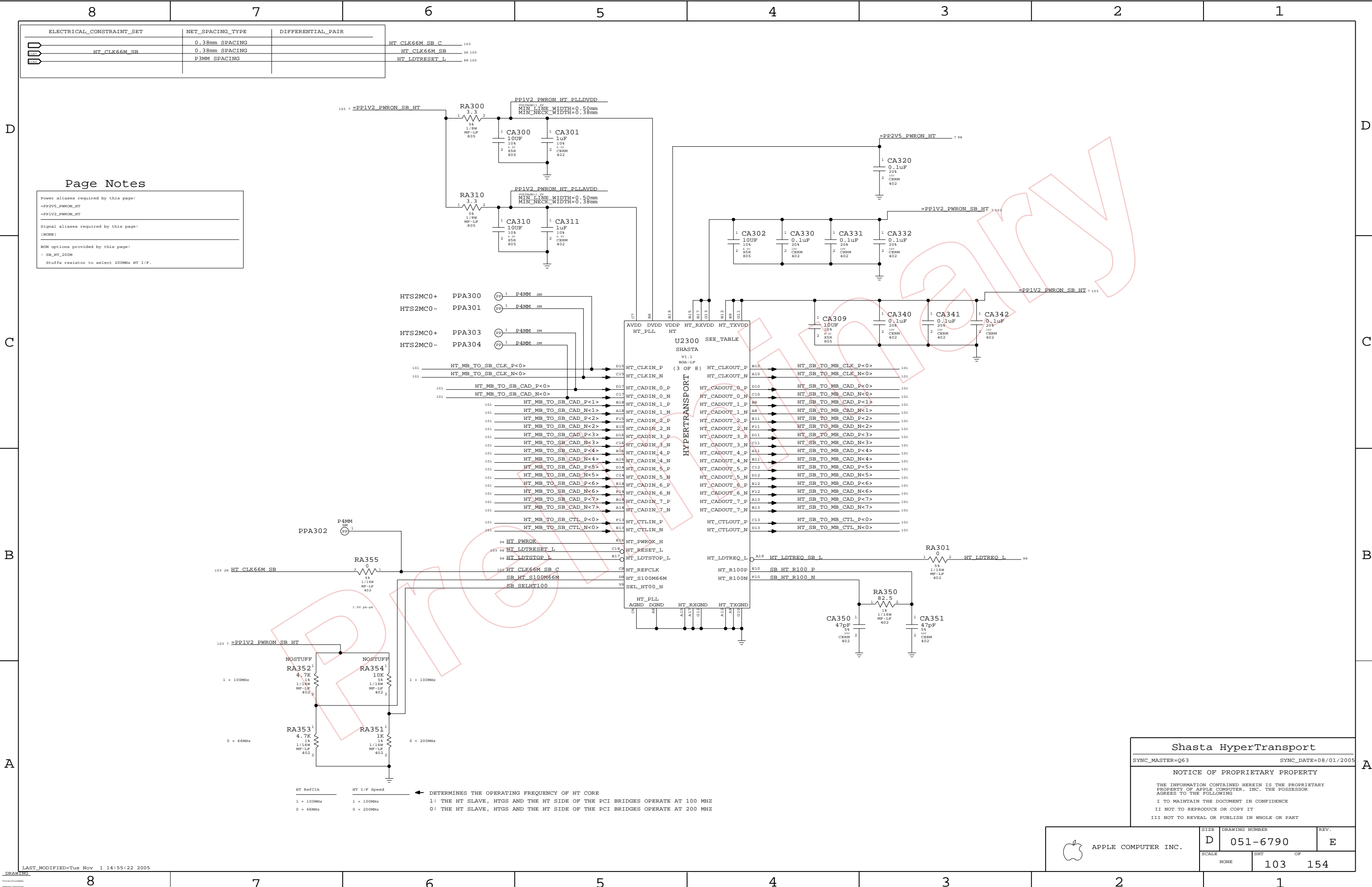




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HT ALIASES	
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 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6790	REV. E
	SCALE NONE	SHT 101 OF 154	



Page Notes

Power aliases required by this page:  
=PP2V5\_PWRON\_HT  
=PP1V2\_PWRON\_HT

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
- SB\_HT\_200M

Stuffs resistor to select 200MHz HT I/F.

Shasta HyperTransport

SYNC\_MASTER=Q63

SYNC\_DATE=08/01/2005

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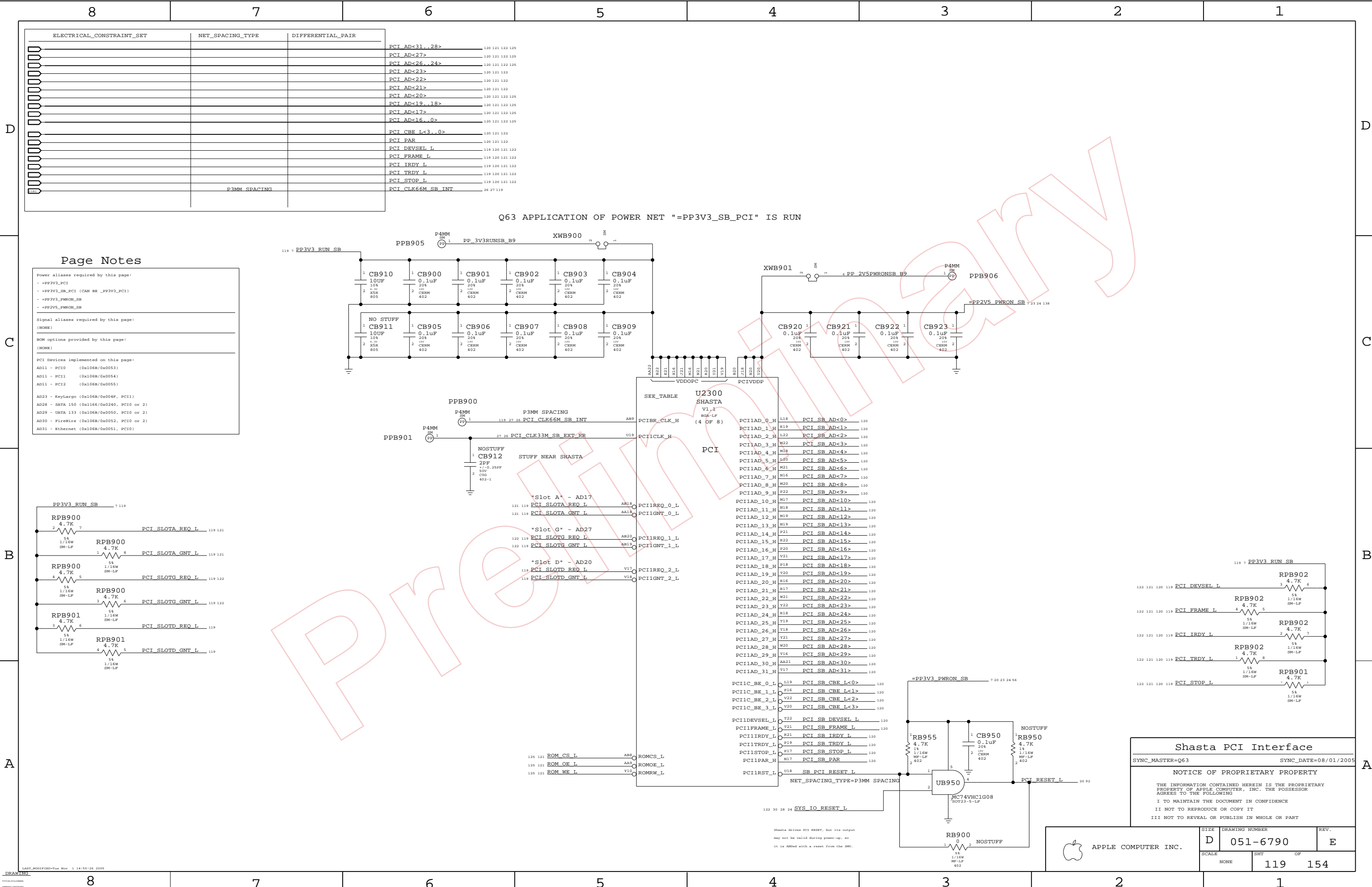
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	E
SCALE	SHT OF		
	NONE	103	154





Page Notes

Power aliases required by this page:

- PP3V3\_PCI
- PP3V3\_SB\_PCI (CAN BE PP3V3\_PCI)
- PP3V3\_PWRON\_SB
- PP2V5\_PWRON\_SB

Signal aliases required by this page:

(NONE)

ROM options provided by this page:

(NONE)

PCI Devices implemented on this page:

- AD11 - PCI0 (0x106B/0x0053)
- AD11 - PCI1 (0x106B/0x0054)
- AD11 - PCI2 (0x106B/0x0055)
- AD23 - KeyLargo (0x106B/0x004F, PCI1)
- AD28 - SATA 150 (0x1166/0x0240, PCI0 or 2)
- AD29 - UATA 133 (0x106B/0x0050, PCI0 or 2)
- AD30 - FireWire (0x106B/0x0052, PCI0 or 2)
- AD31 - Ethernet (0x106B/0x0051, PCI0)

Shasta PCI Interface

SYNC\_MASTER=Q63 SYNC\_DATE=08/01/2005

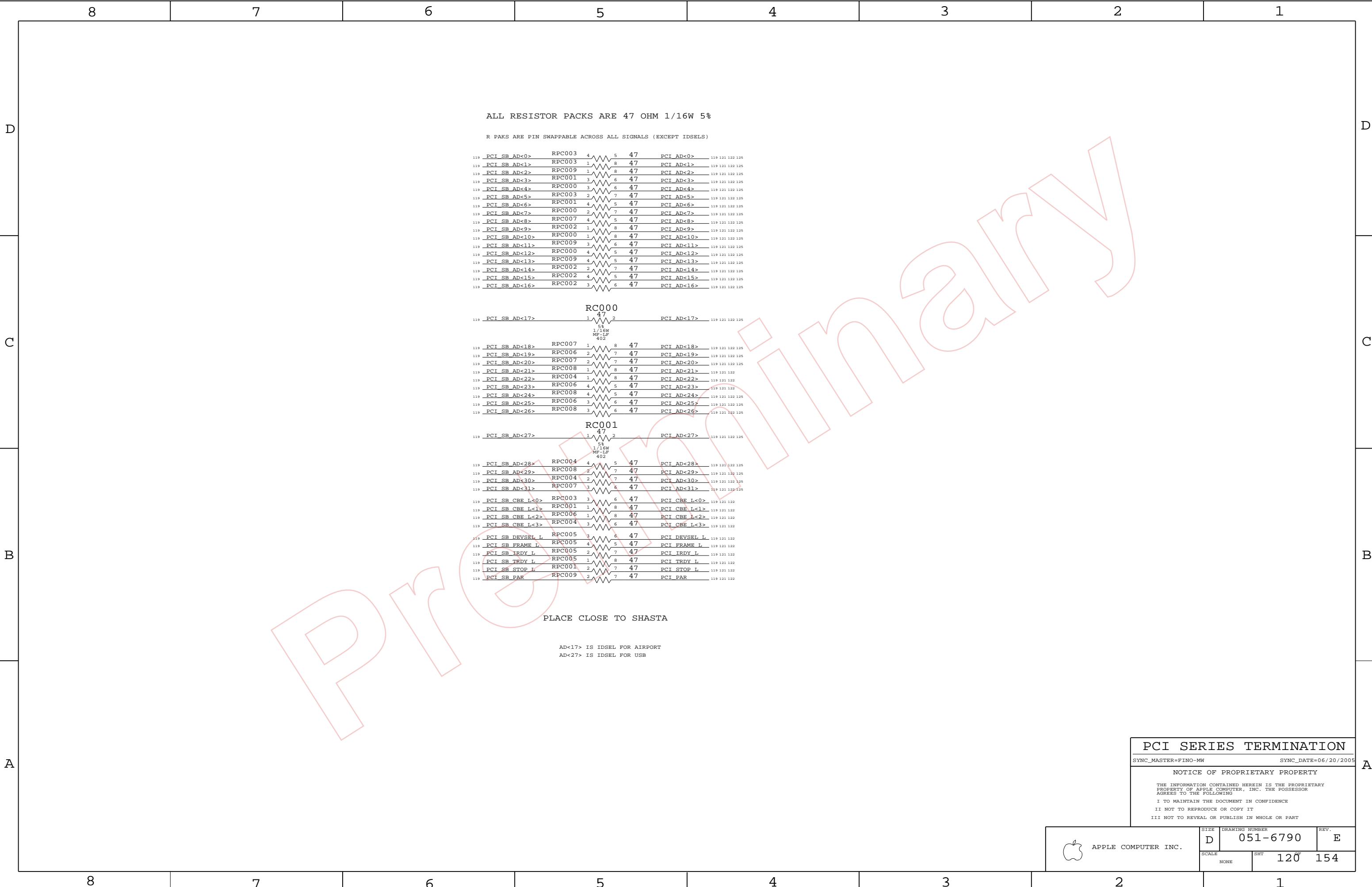
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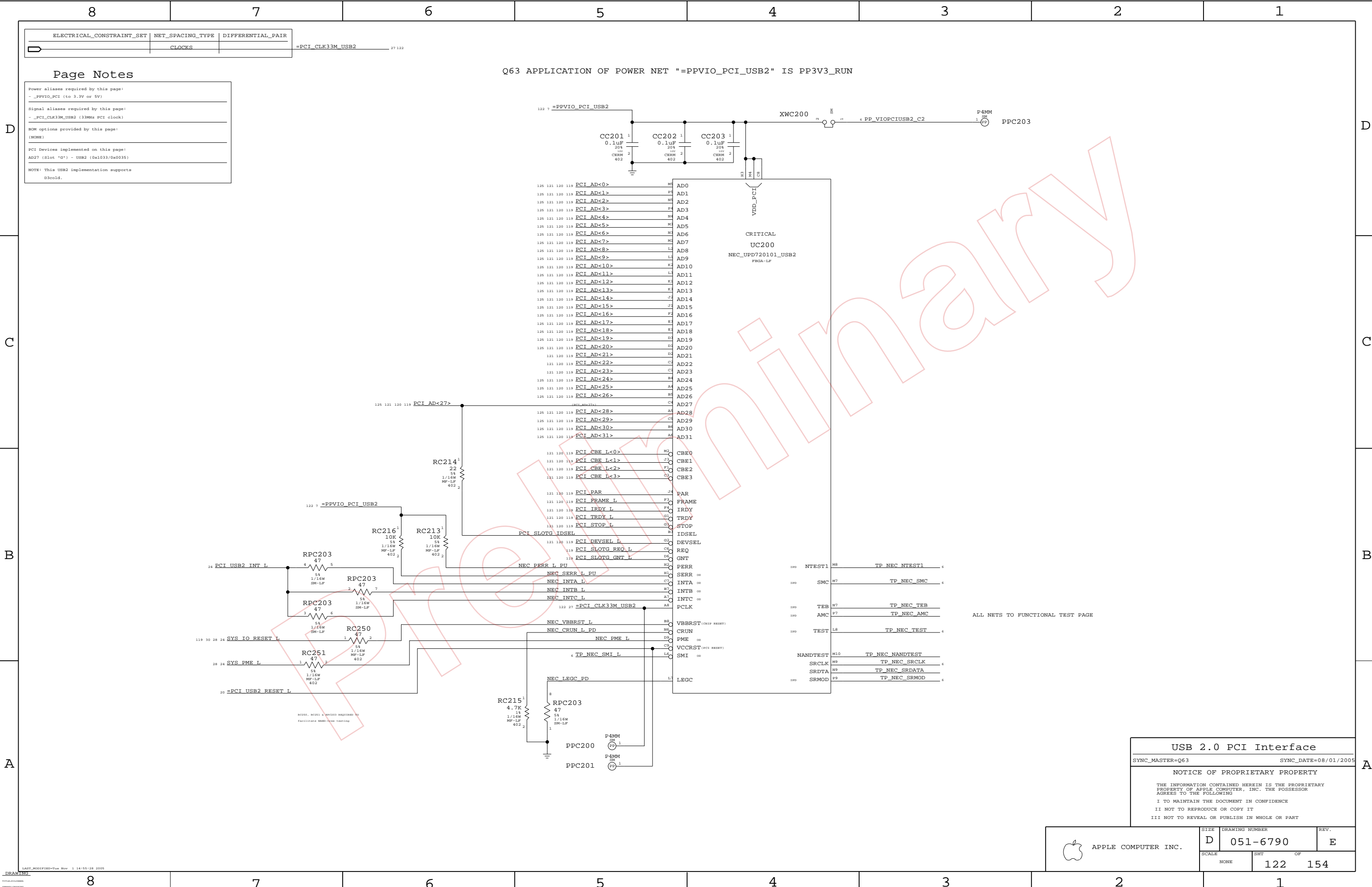


APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE	SHT	OF
NONE	119	154







ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	CLOCKS	
=PCI_CLK33M_USB2		27 122

Page Notes

Power aliases required by this page:  
- \_PPVIO\_PCI (to 3.3V or 5V)

Signal aliases required by this page:  
- \_PCI\_CLK33M\_USB2 (33MHz PCI clock)

BOM options provided by this page:  
(NONE)

PCI Devices implemented on this page:  
AD27 (slot "G") - USB2 (0x1033/0x0035)

NOTE: This USB2 implementation supports D3cold.

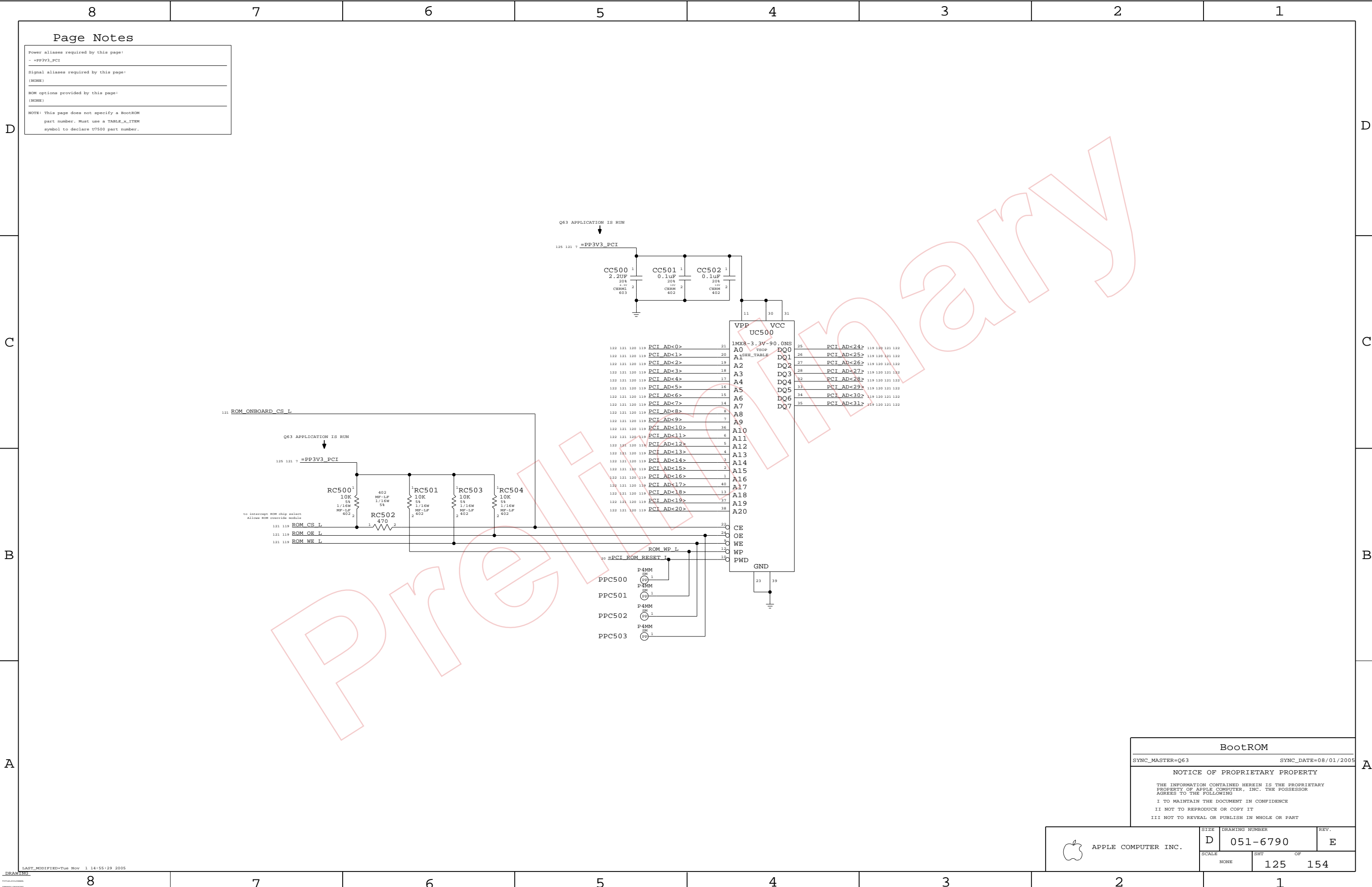
Q63 APPLICATION OF POWER NET "=PPVIO\_PCI\_USB2" IS PP3V3\_RUN

ALL NETS TO FUNCTIONAL TEST PAGE

USB 2.0 PCI Interface	
SYNC_MASTER=Q63	SYNC_DATE=08/01/2005
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	E
SCALE		SHT	OF
NONE		122	154





Page Notes

Power aliases required by this page:  
- =PP3V3\_PCI

Signal aliases required by this page:  
(NONE)

ROM options provided by this page:  
(NONE)

NOTE: This page does not specify a BootROM part number. Must use a TABLE\_X\_ITEM symbol to declare U7500 part number.

BootROM

SYNC\_MASTER=Q63 SYNC\_DATE=08/01/2005

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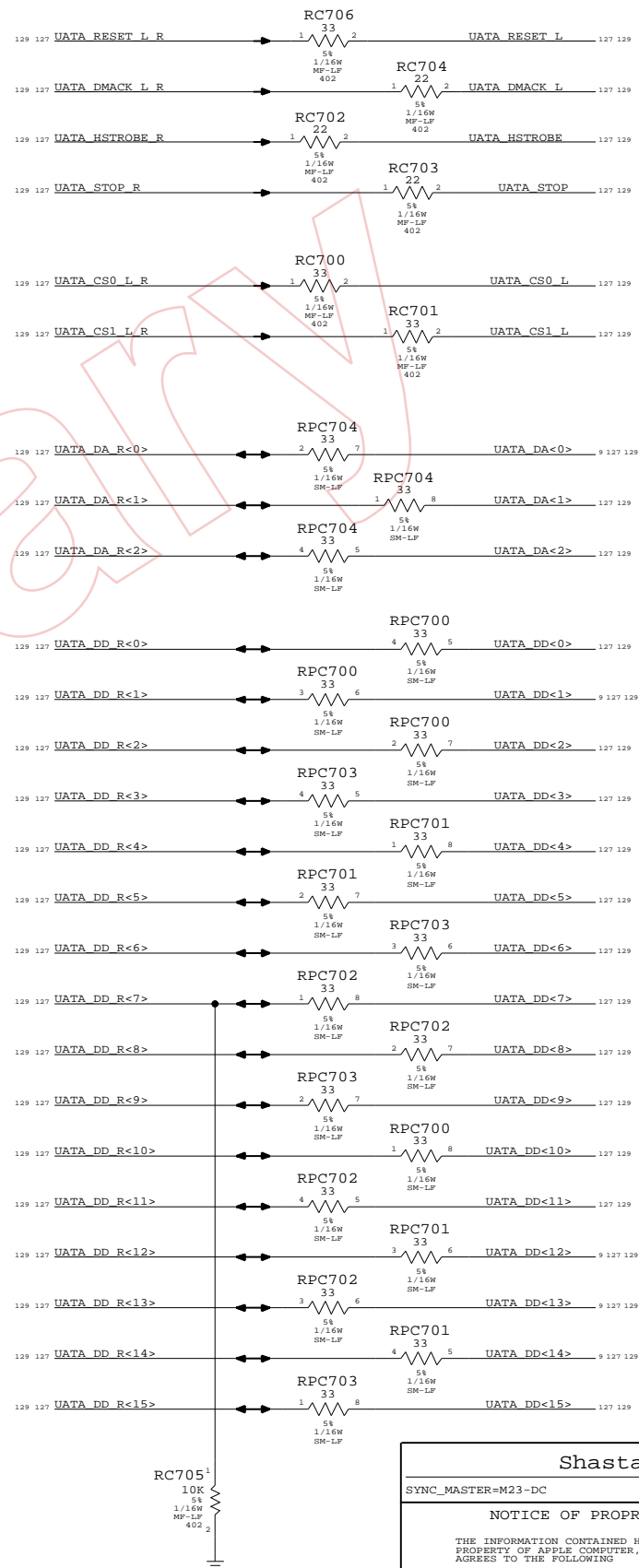
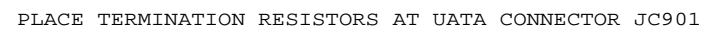
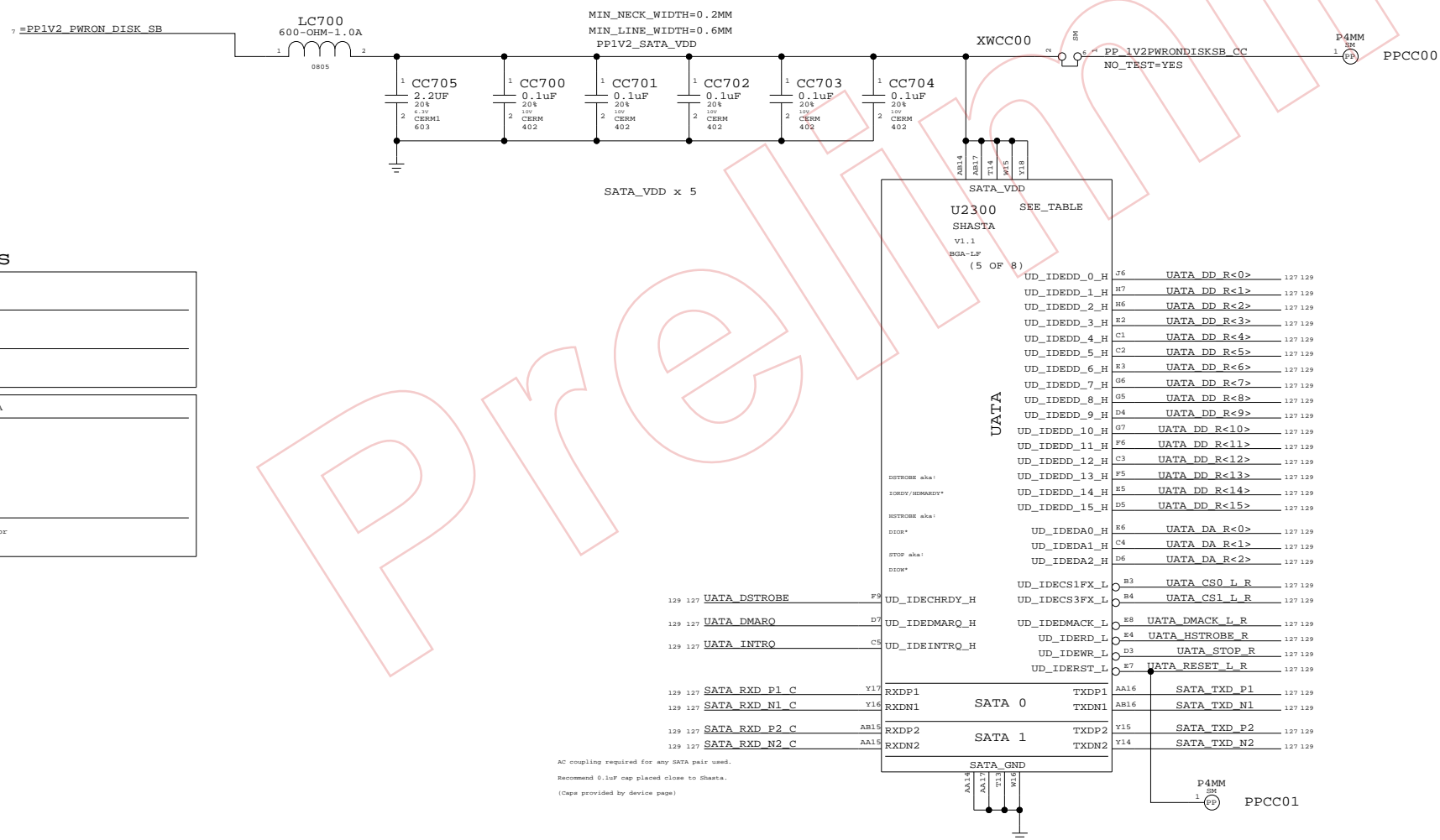
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	E
SCALE		SHT	OF
NONE		125	154

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR		
	SATA	SATA	SATA_RXD1_C	SATA_RXD_P1_C	127 129
	SATA	SATA	SATA_RXD1_C	SATA_RXD_N1_C	127 129
	SATA	SATA	SATA_TXD1	SATA_TXD_P1	127 129
	SATA	SATA	SATA_TXD1	SATA_TXD_N1	127 129
	SATA	SATA	SATA_RXD2_C	SATA_RXD_P2_C	127 129
	SATA	SATA	SATA_RXD2_C	SATA_RXD_N2_C	127 129
	SATA	SATA	SATA_TXD2	SATA_TXD_P2	127 129
	SATA	SATA	SATA_TXD2	SATA_TXD_N2	127 129
				UATA_DD<15..8>	9 127 129
				UATA_DD<7>	127 129
				UATA_DD<6..0>	9 127 129
				UATA_DA<2..0>	9 127 129
				UATA_CS0_L	127 129
				UATA_CS1_L	127 129
				UATA_HSTROBE	127 129
				UATA_STOP	127 129
	UATA_NETSPA			UATA_DMACK_L	127 129
				UATA_RESET_L	127 129
				UATA_DSTROBE	127 129
				UATA_DMARQ	127 129
				UATA_INTRO	127 129
				UATA_DD_R<15..8>	127 129
				UATA_DD_R<7>	127 129
				UATA_DD_R<6..0>	127 129
				UATA_DA_R<2..0>	127 129
				UATA_CS0_L_R	127 129
				UATA_CS1_L_R	127 129
				UATA_DMACK_L_R	127 129
				UATA_HSTROBE_R	127 129
				UATA_STOP_R	127 129
				UATA_RESET_L_R	127 129



Page Notes

Power aliases required by this page:

- `_PP1V2_PWRON_DISK`

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
(NONE)

Net Spacing Type: SATA

Line To Line: 0.38mm  
Length Tolerance: 1.27mm  
Primary Max Sep: 0.25mm outer  
Primary Max Sep: 0.23mm inner  
Secondary Max Sep: 2.54mm  
Secondary Length: 12.70mm

NOTE: Target differential impedance for  
SATA data pairs is 100 ohms.

Shasta Disk

SYNC\_MASTER=M23-DC

SYNC\_DATE=06/20/2005

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APPLE COMPUTER INC.

	SIZE
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DRAWING NUMBER
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REV.

SCALE	

SHT

1

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154

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ENET SERIES TERM

SYNC\_MASTER=FINO-DC

SYNC\_DATE=06/20/2005


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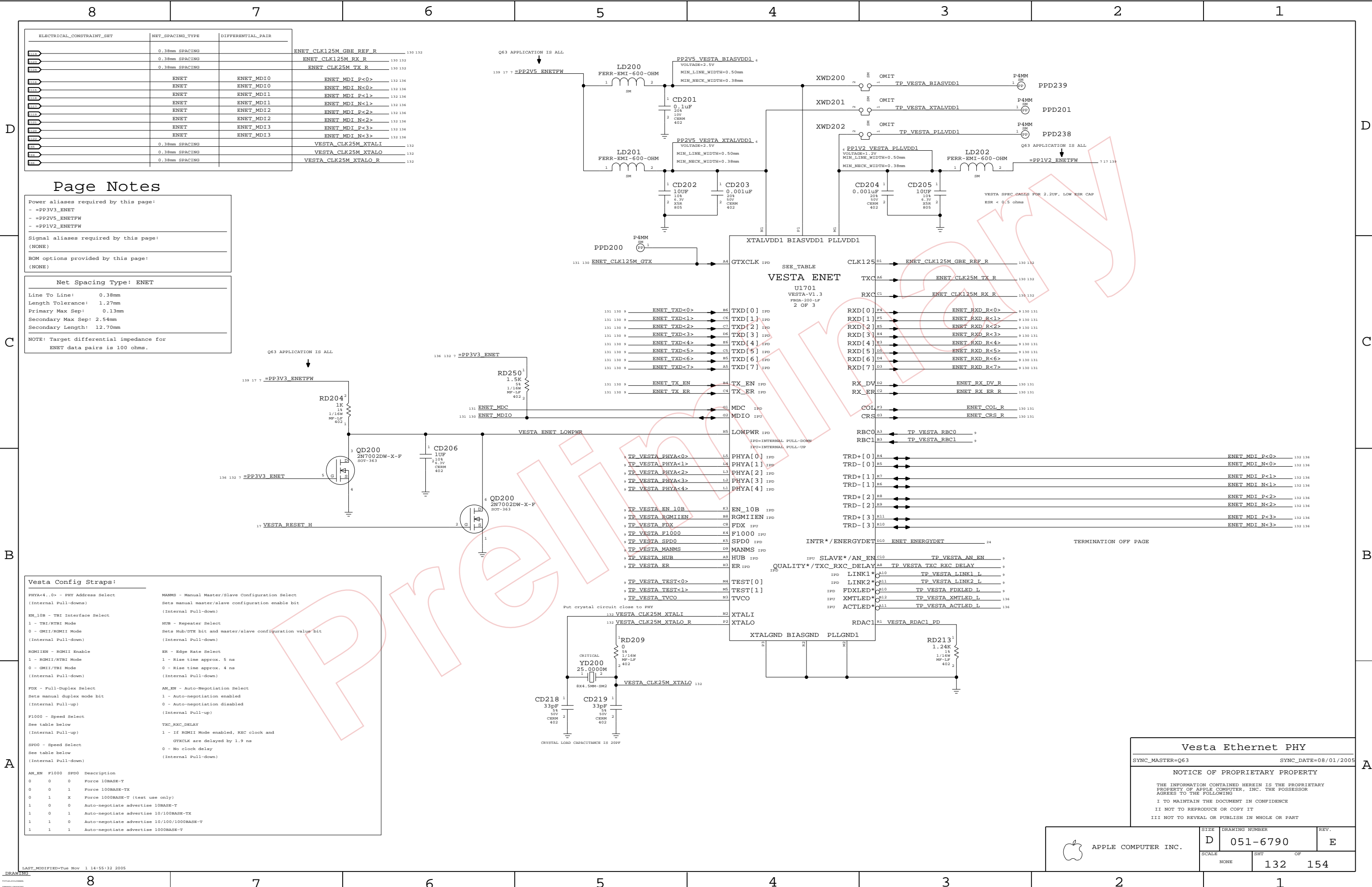
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 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6790	REV. E
	SCALE NONE	SHT 130	154







Page Notes

Power aliases required by this page:

- =PP3V3\_ENET
- =PP2V5\_ENETFW
- =PP1V2\_ENETFW

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

Net Spacing Type: ENET

Line To Line: 0.38mm

Length Tolerance: 1.27mm

Primary Max Sep: 0.13mm

Secondary Max Sep: 2.54mm

Secondary Length: 12.70mm

NOTE: Target differential impedance for ENET data pairs is 100 ohms.

Vesta Config Straps:			
PHYA<4..0> - PHY Address Select (Internal Pull-downs)			
EN_10B - TBI Interface Select 1 - TBI/RTBI Mode 0 - GMII/RGMII Mode (Internal Pull-down)			
RGMIIEN - RGMII Enable 1 - RGMII/RTBI Mode 0 - GMII/TBI Mode (Internal Pull-down)			
FDX - Full-Duplex Select Sets manual duplex mode bit (Internal Pull-up)			
F1000 - Speed Select See table below (Internal Pull-up)			
SPD0 - Speed Select See table below (Internal Pull-down)			
AN_EN F1000 SPD0 Description			
0	0	0	Force 10BASE-T
0	0	1	Force 100BASE-TX
0	1	X	Force 1000BASE-T (test use only)
1	0	0	Auto-negotiate advertise 10BASE-T
1	0	1	Auto-negotiate advertise 10/100BASE-TX
1	1	0	Auto-negotiate advertise 10/100/1000BASE-T
1	1	1	Auto-negotiate advertise 1000BASE-T

Vesta Ethernet PHY

SYNC\_MASTER=Q63 SYNC\_DATE=08/01/2005

NOTICE OF PROPRIETARY PROPERTY

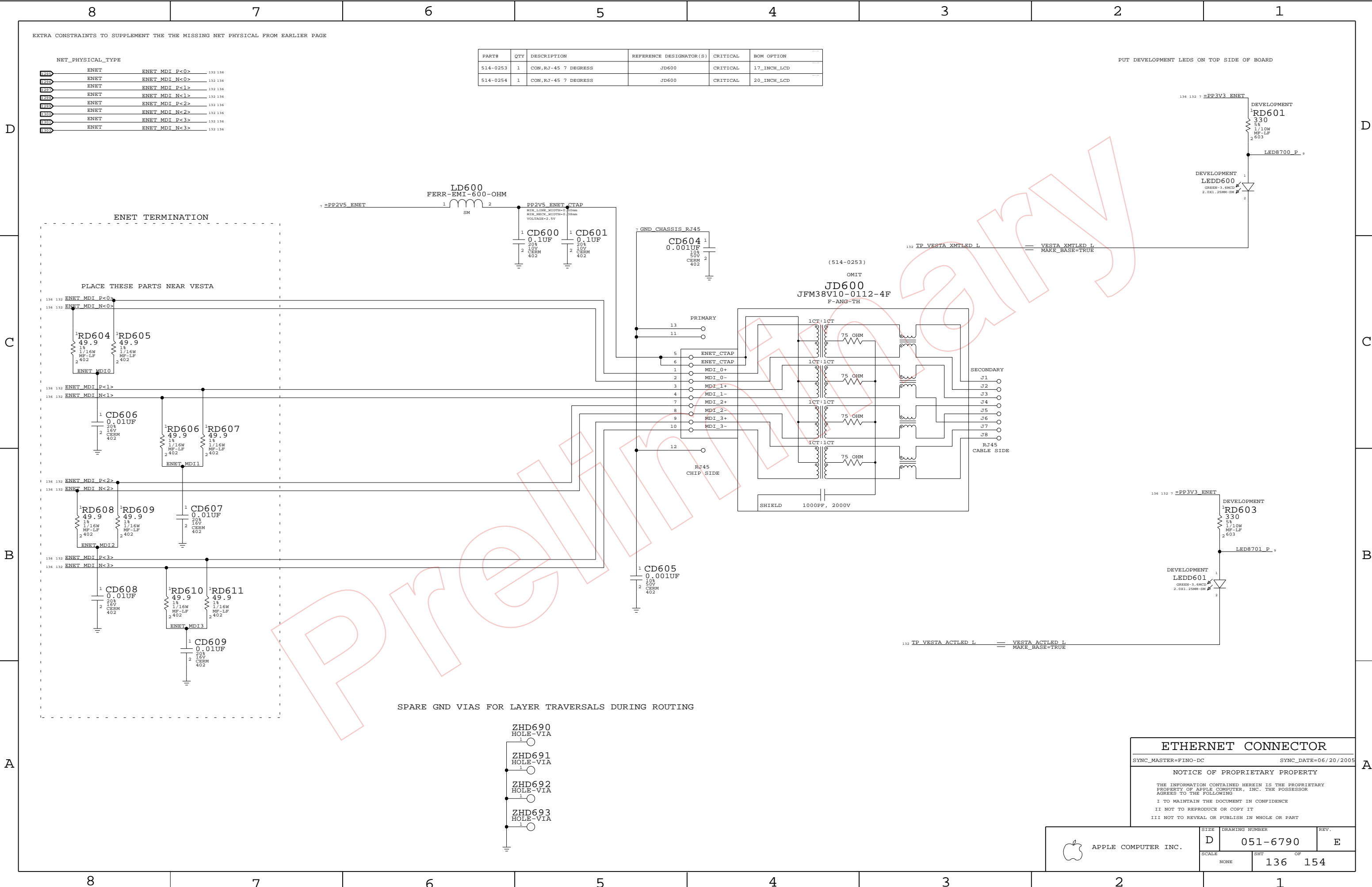
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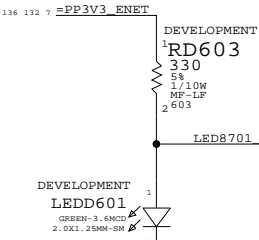
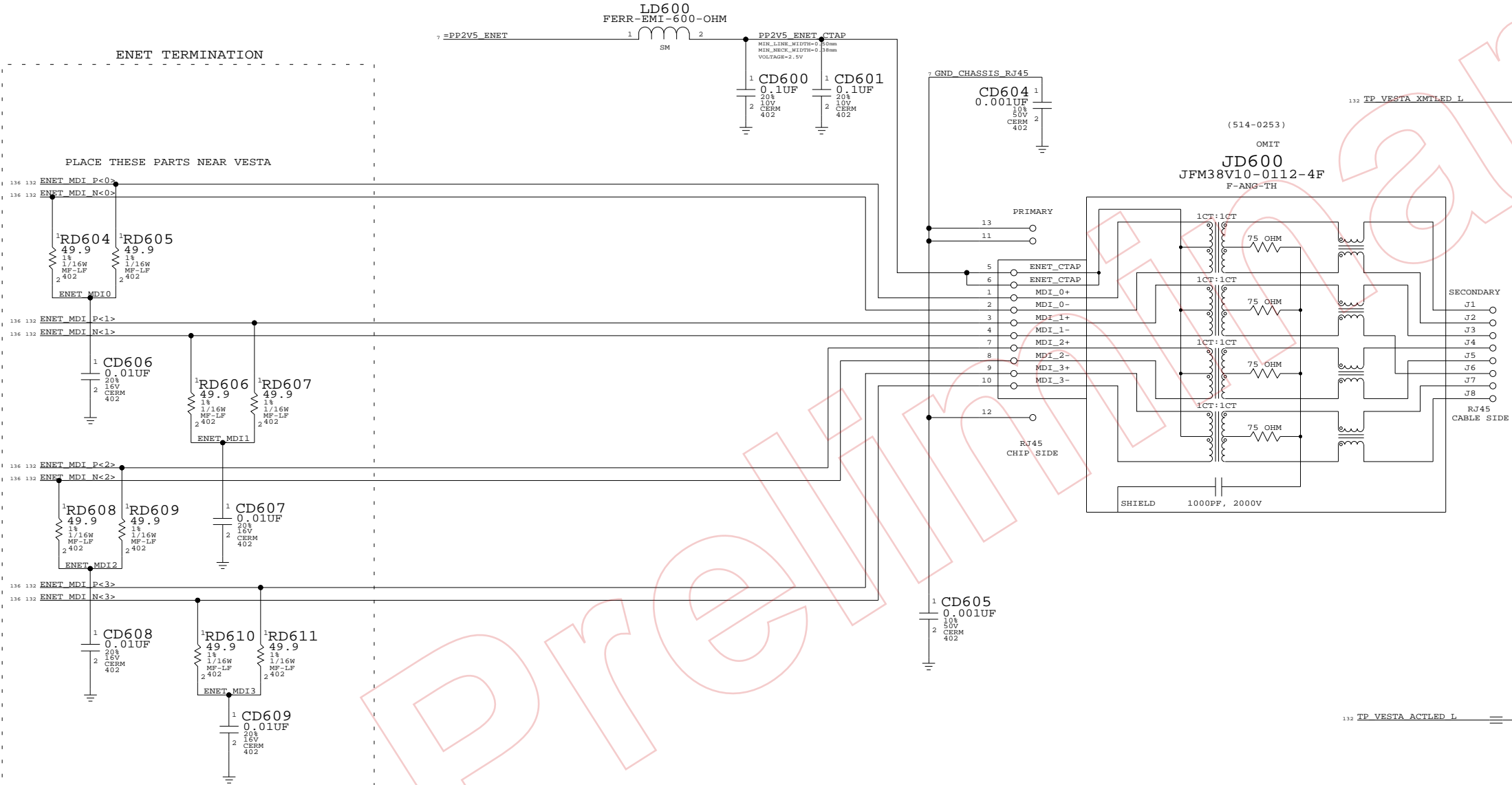
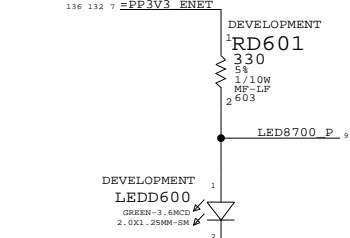
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6790	REV. E
	SCALE NONE	SHT 132	OF 154



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0253	1	CON,RJ-45 7 DEGRESS	JD600	CRITICAL	17_INCH_LCD
514-0254	1	CON,RJ-45 7 DEGRESS	JD600	CRITICAL	20_INCH_LCD

NET_PHYSICAL_TYPE		
ENET	ENET MDI P<0>	132 136
ENET	ENET MDI N<0>	132 136
ENET	ENET MDI P<1>	132 136
ENET	ENET MDI N<1>	132 136
ENET	ENET MDI P<2>	132 136
ENET	ENET MDI N<2>	132 136
ENET	ENET MDI P<3>	132 136
ENET	ENET MDI N<3>	132 136

PUT DEVELOPMENT LEDS ON TOP SIDE OF BOARD



ETHERNET CONNECTOR	
SYNC_MASTER=FINO-DC	SYNC_DATE=06/20/2005
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	E
SCALE		SHT	OF
NONE		136	154





D

## C

**R**

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DRAWING



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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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D	051 6700	1
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D	051-6790	1
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SCALE	SHT	OF
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NONE	139	154
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[illegible]





## Page Notes

Power aliases required by this page:

- \_PP5V\_PWRON\_USB
- \_PP5V\_PWRON\_UDASH
- \_PP3V3\_PWRON\_UDASH
- \_PP3V3\_PWRON\_BT

Signal aliases required by this page:  
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the USB pairs to their appropriate destinations and/or to properly terminate unused signals.

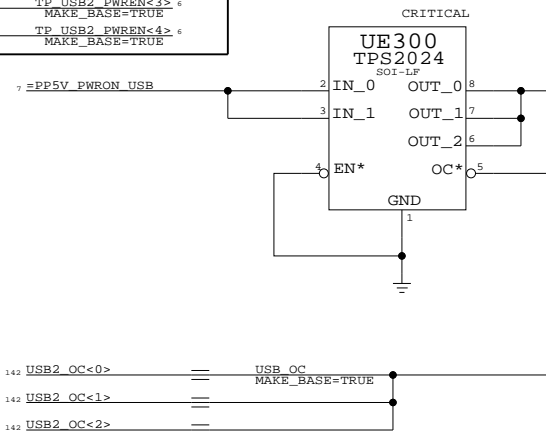
BOM options provided by this page:  
(NONE)

NOTE: USB pairs are NOT constrained on this page. It is assumed that the USB Host Controller page will provide the appropriate constraints to apply to entire USB D+/D- XNets.

### neoBorg Implementation

NOTE: This design does not provide power control on USB ports 2-4. Rename USB controller outputs to indicate single-pin connections.

142 USB2_PWREN<0>	==	TP_USB2_PWREN<0>	6
142 USB2_PWREN<1>	==	TP_USB2_PWREN<1>	6
142 USB2_PWREN<2>	==	TP_USB2_PWREN<2>	6
142 USB2_PWREN<3>	==	TP_USB2_PWREN<3>	6
142 USB2_PWREN<4>	==	TP_USB2_PWREN<4>	6

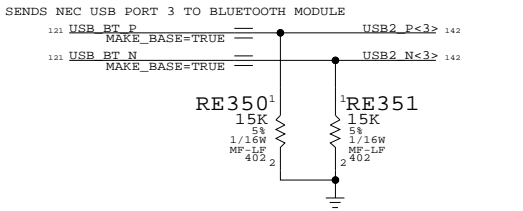
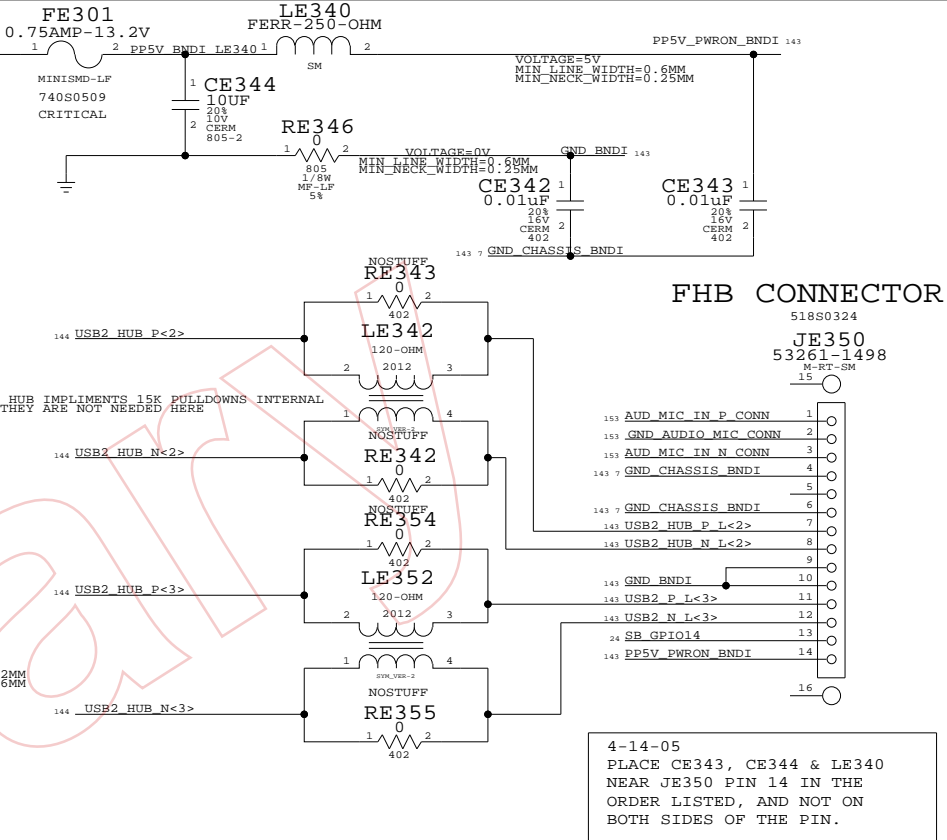
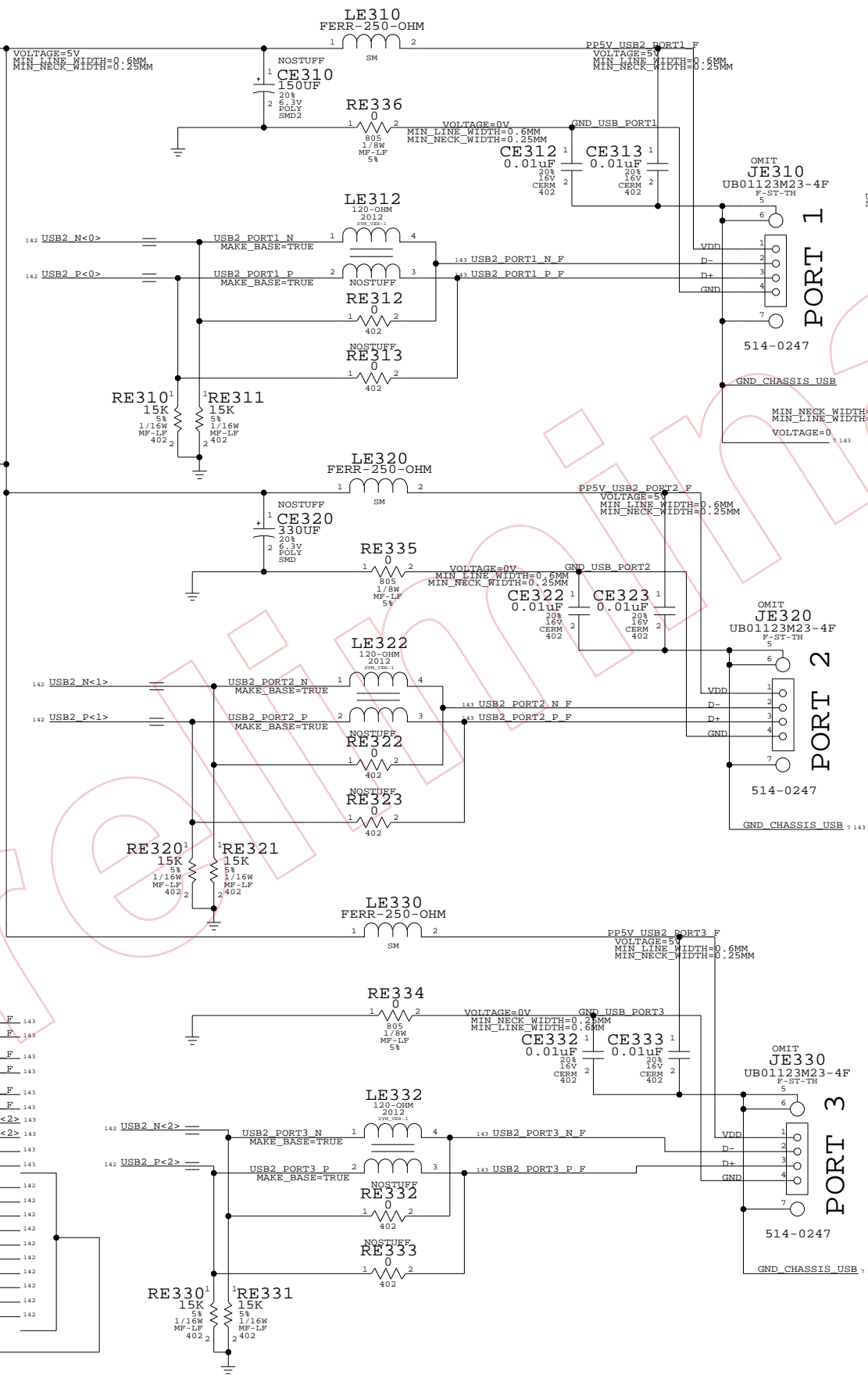


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0294	3	USB RECEPTACLE,4P,UB1123-M23B-4F	JE310,JE320,JE330	CRITICAL	17_INCH_LCD
514-0295	3	USB RECEPTACLE,4P,UB1123-M33B-4F	JE310,JE320,JE330	CRITICAL	20_INCH_LCD

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE
PROVIDED BY	USB2	USB2_PORT1_P	USB2
USB CONTROLLER	USB2	USB2_PORT1_F	USB2
	USB2	USB2_PORT2_P	USB2
	USB2	USB2_PORT2_F	USB2
	USB2	USB2_PORT3_P	USB2
	USB2	USB2_PORT3_F	USB2
	USB2	USB2_HUB_P	USB2
	USB2	USB2_HUB_F	USB2
	USB2	USB2_BNDI_F	USB2
	USB2	USB2_BNDI_F	USB2
	USB2	USB2_0_IC	USB2
	USB2	USB2_0_IC	USB2
	USB2	USB2_1_IC	USB2
	USB2	USB2_1_IC	USB2
	USB2	USB2_2_IC	USB2
	USB2	USB2_2_IC	USB2
	USB2	USB2_3_IC	USB2
	USB2	USB2_3_IC	USB2
	USB2	USB2_4_IC	USB2
	USB2	USB2_4_IC	USB2

DUE TO THESE NETS ARE ON A Q63 SHARED PAGE 124, THESE PROPERTIES FOR M23/M33 WERE PLACED ON THIS PAGE.

## External USB Ports



## USB Device Interfaces

SYNC\_MASTER=FINO-PC SYNC\_DATE=06/20/2005

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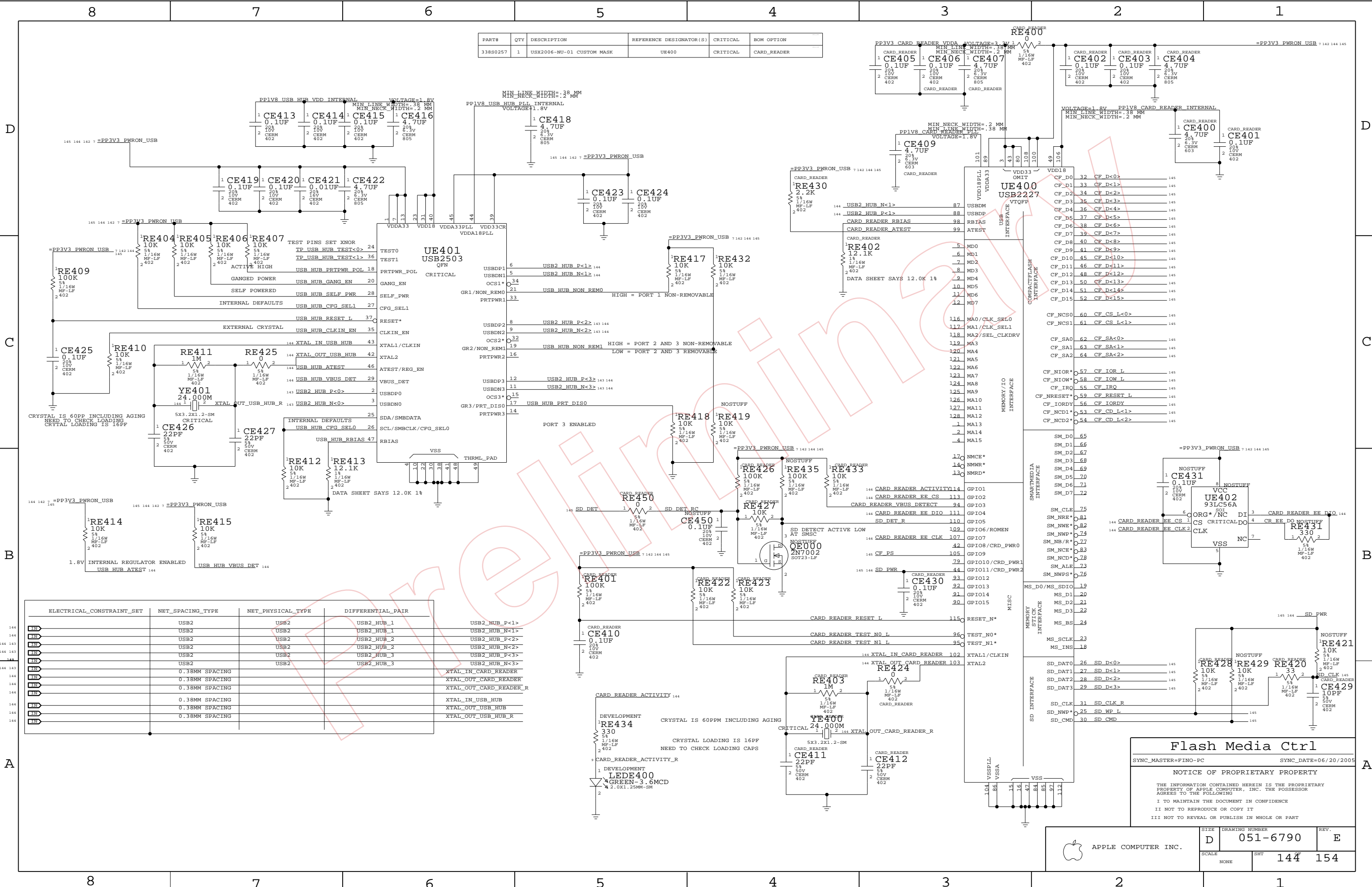
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SCALE	SIT	OF
NONE	143	154





PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0257	1	USX2006-NU-01 CUSTOM MASK	UE400	CRITICAL	CARD_READER

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR
IN	USB2	USB2	USB2_HUB_1
IN	USB2	USB2	USB2_HUB_2
IN	USB2	USB2	USB2_HUB_3
IN	USB2	USB2	USB2_HUB_4
IN	0.38MM SPACING	0.38MM SPACING	XTAL_IN_CARD_READER
IN	0.38MM SPACING	0.38MM SPACING	XTAL_OUT_CARD_READER
IN	0.38MM SPACING	0.38MM SPACING	XTAL_IN_USB_HUB
IN	0.38MM SPACING	0.38MM SPACING	XTAL_OUT_USB_HUB
IN	0.38MM SPACING	0.38MM SPACING	XTAL_IN_CARD_READER_R
IN	0.38MM SPACING	0.38MM SPACING	XTAL_OUT_CARD_READER_R
IN	0.38MM SPACING	0.38MM SPACING	XTAL_IN_USB_HUB_R
IN	0.38MM SPACING	0.38MM SPACING	XTAL_OUT_USB_HUB_R

Flash Media Ctrl

SYNC\_MASTER=FINO-PC      SYNC\_DATE=06/20/2005

NOTICE OF PROPRIETARY PROPERTY

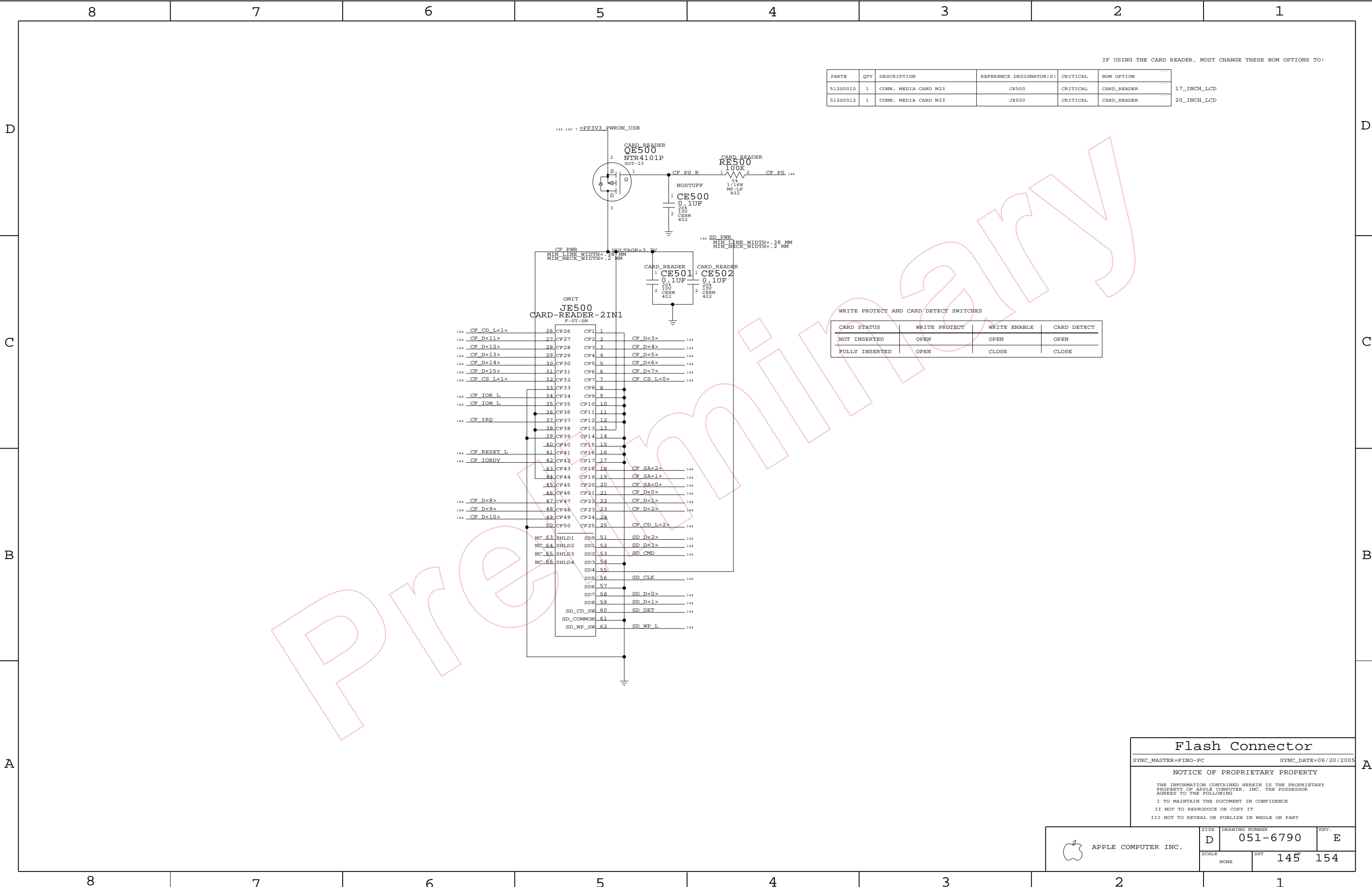
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IF USING THE CARD READER, MUST CHANGE THESE BOM OPTIONS TO:					
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
51280010	1	CONN, MEDIA CARD M23	JE500	CRITICAL	CARD_READER
51280012	1	CONN, MEDIA CARD M33	JE500	CRITICAL	CARD_READER

17\_INCH\_LCD  
20\_INCH\_LCD

WRITE PROTECT AND CARD DETECT SWITCHES			
CARD STATUS	WRITE PROTECT	WRITE ENABLE	CARD DETECT
NOT INSERTED	OPEN	OPEN	OPEN
FULLY INSERTED	OPEN	CLOSE	CLOSE

Flash Connector

SYNC\_MASTER=FINO-PCSYNC\_DATE=06/20/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	E
SCALE		SHT	145 OF 154
NONE			

D

C

B

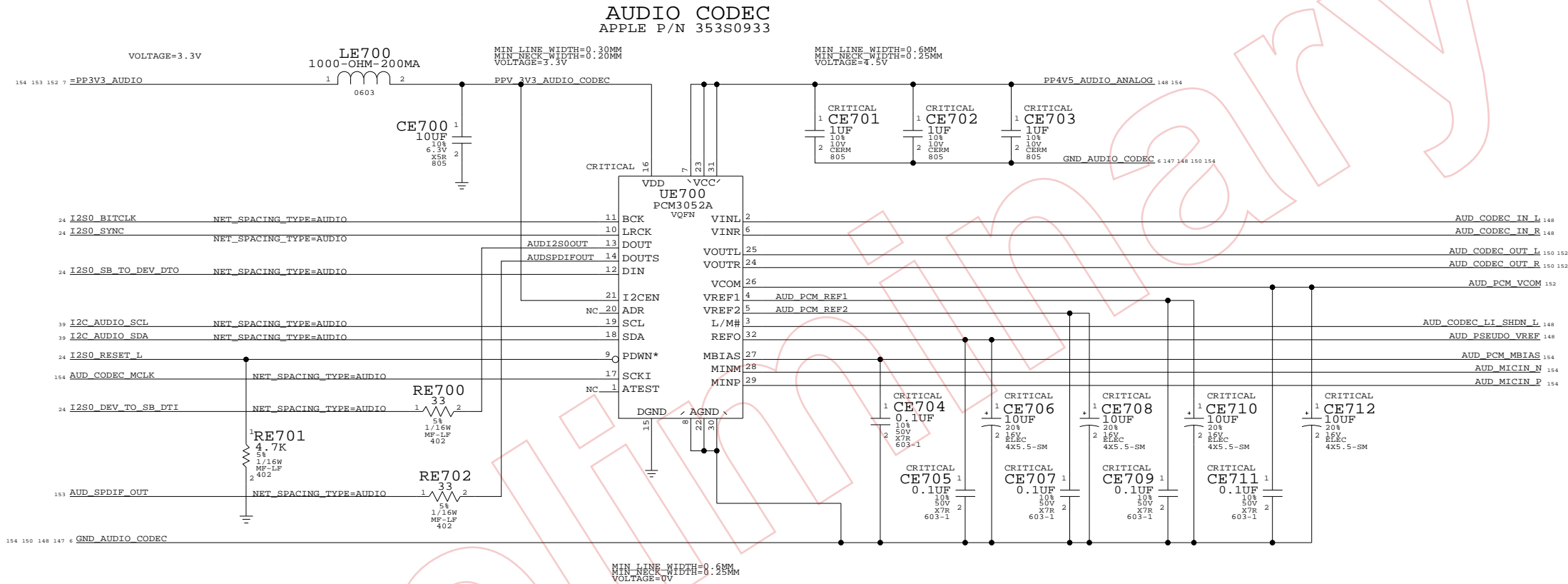
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**AUDIO: CODEC**

SYNC\_MASTER=FINO-SO SYNC\_DATE=10/07/2005

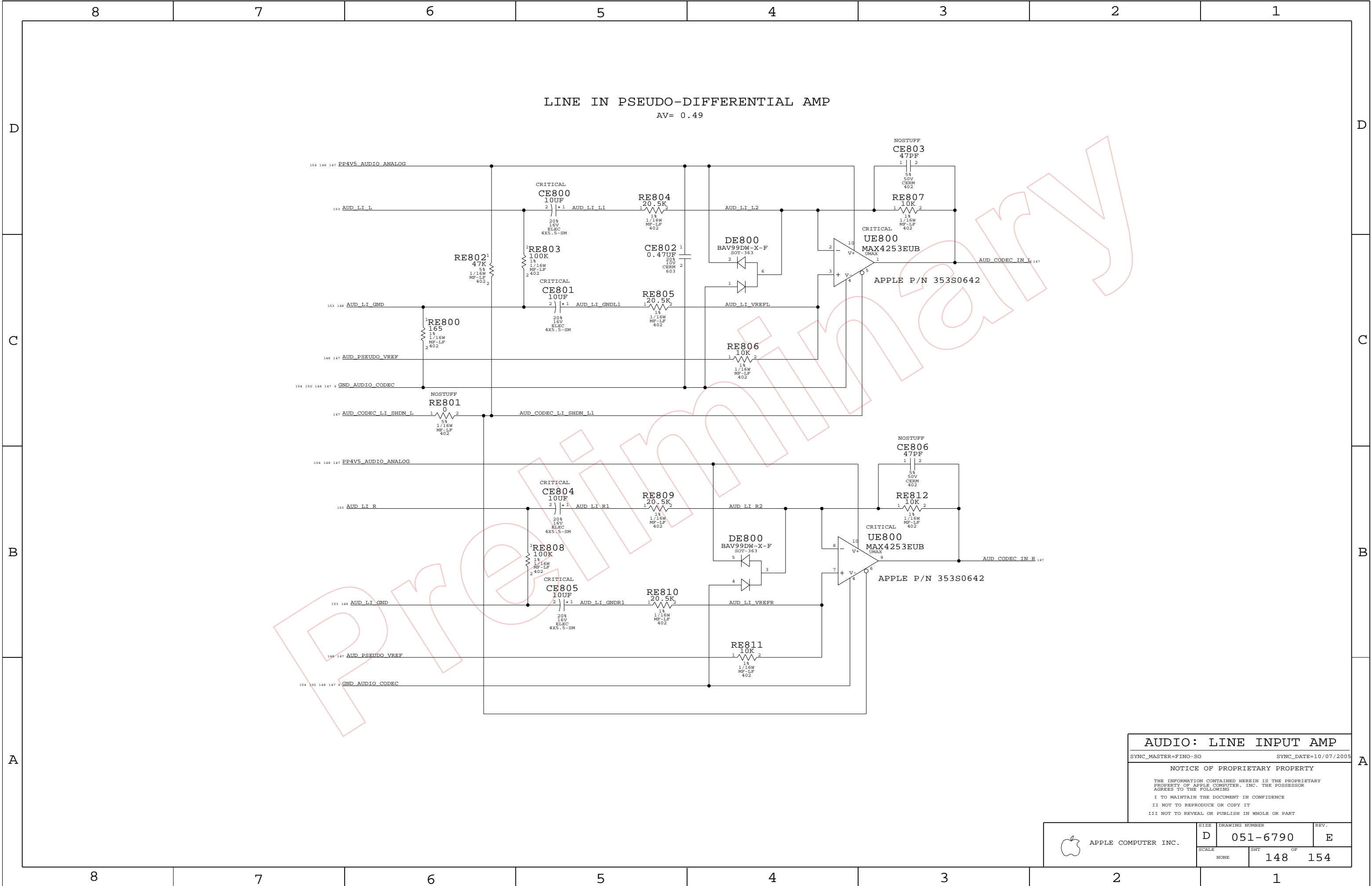
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D	051-6790	E
SCALE	SHT	OF
NONE	147	154



AUDIO: LINE INPUT AMP

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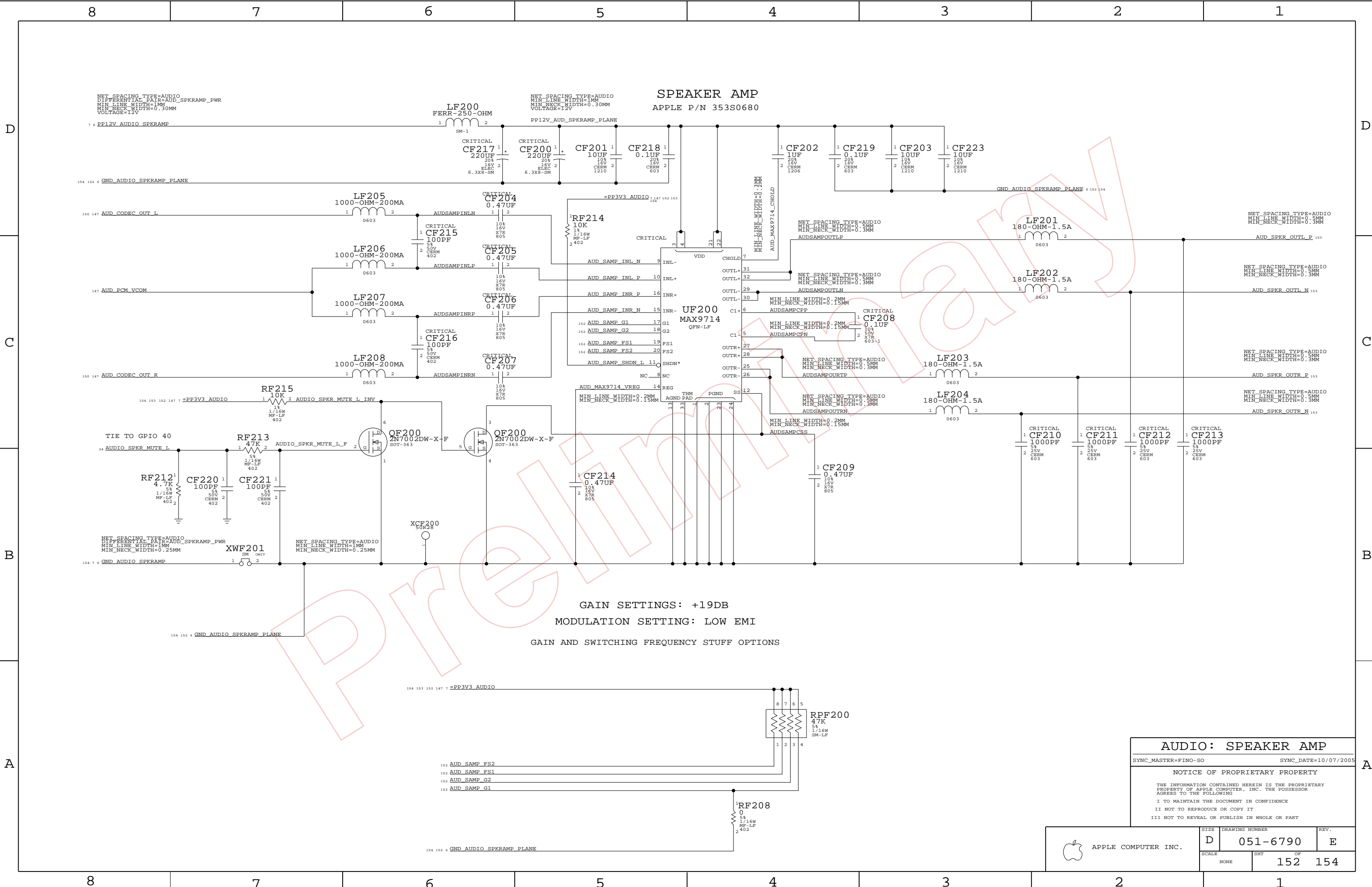


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SIZE	DRAWING NUMBER	REV.
D	051-6790	E
SCALE	SHT	OF
NONE	148	154







**AUDIO: SPEAKER AMP**

SYNC\_MASTER=FINO-SO SYNC\_DATE=10/07/2005

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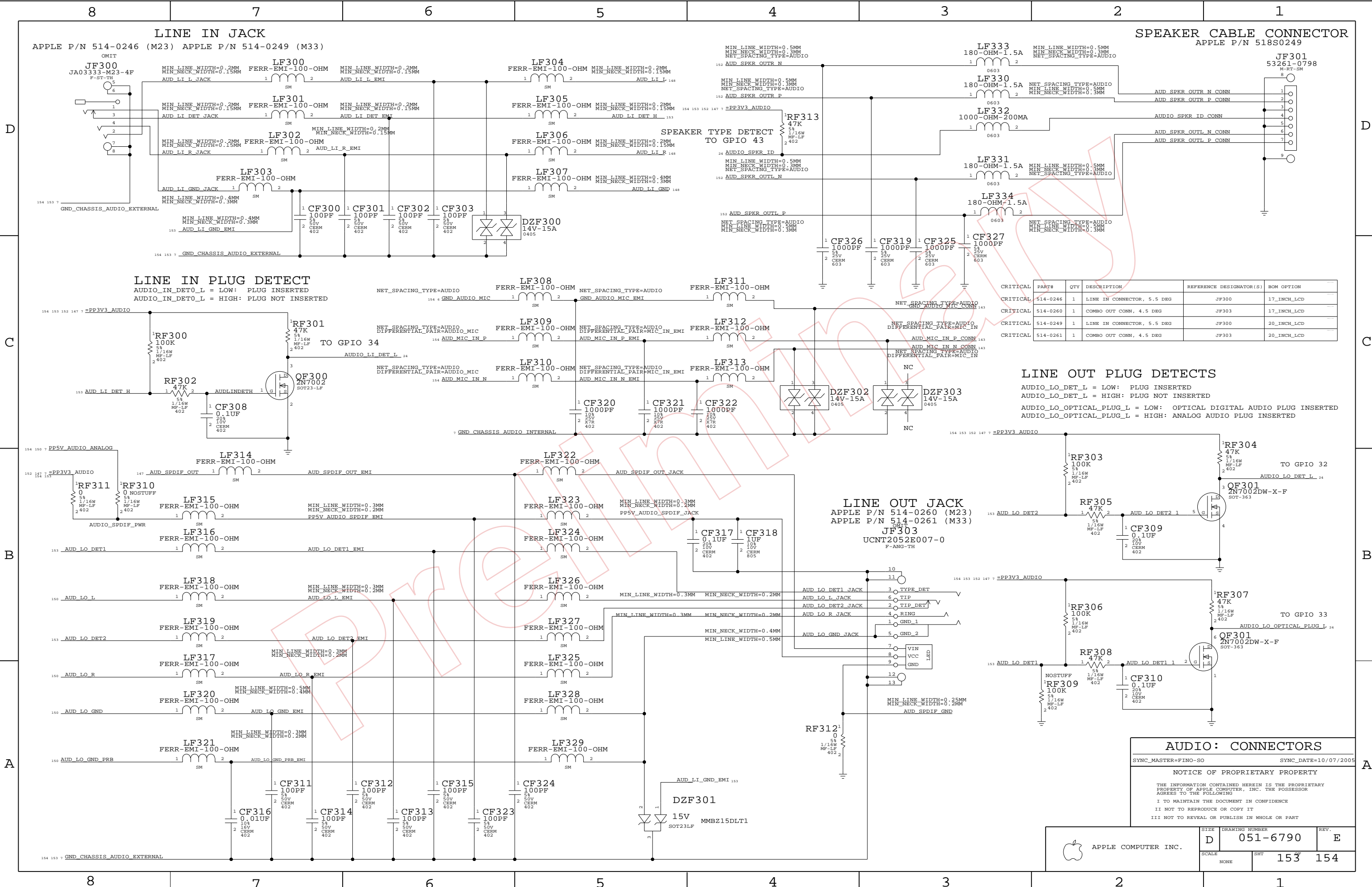
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SCALE	SHT		OF
	NONE		152 154



Critical	Part#	Qty	Description	Reference Designator(s)	BOM Option
CRITICAL	514-0246	1	LINE IN CONNECTOR, 5.5 DEG	JF300	17_INCH_LCD
CRITICAL	514-0260	1	COMBO OUT CONN, 4.5 DEG	JF303	17_INCH_LCD
CRITICAL	514-0249	1	LINE IN CONNECTOR, 5.5 DEG	JF300	20_INCH_LCD
CRITICAL	514-0261	1	COMBO OUT CONN, 4.5 DEG	JF303	20_INCH_LCD

LINE OUT PLUG DETECTS

AUDIO\_LO\_DET\_L = LOW: PLUG INSERTED  
AUDIO\_LO\_DET\_L = HIGH: PLUG NOT INSERTED

AUDIO\_LO\_OPTICAL\_PLUG\_L = LOW: OPTICAL DIGITAL AUDIO PLUG INSERTED  
AUDIO\_LO\_OPTICAL\_PLUG\_L = HIGH: ANALOG AUDIO PLUG INSERTED

AUDIO: CONNECTORS

SYNC\_MASTER=FINO-SO

SYNC\_DATE=10/07/2005

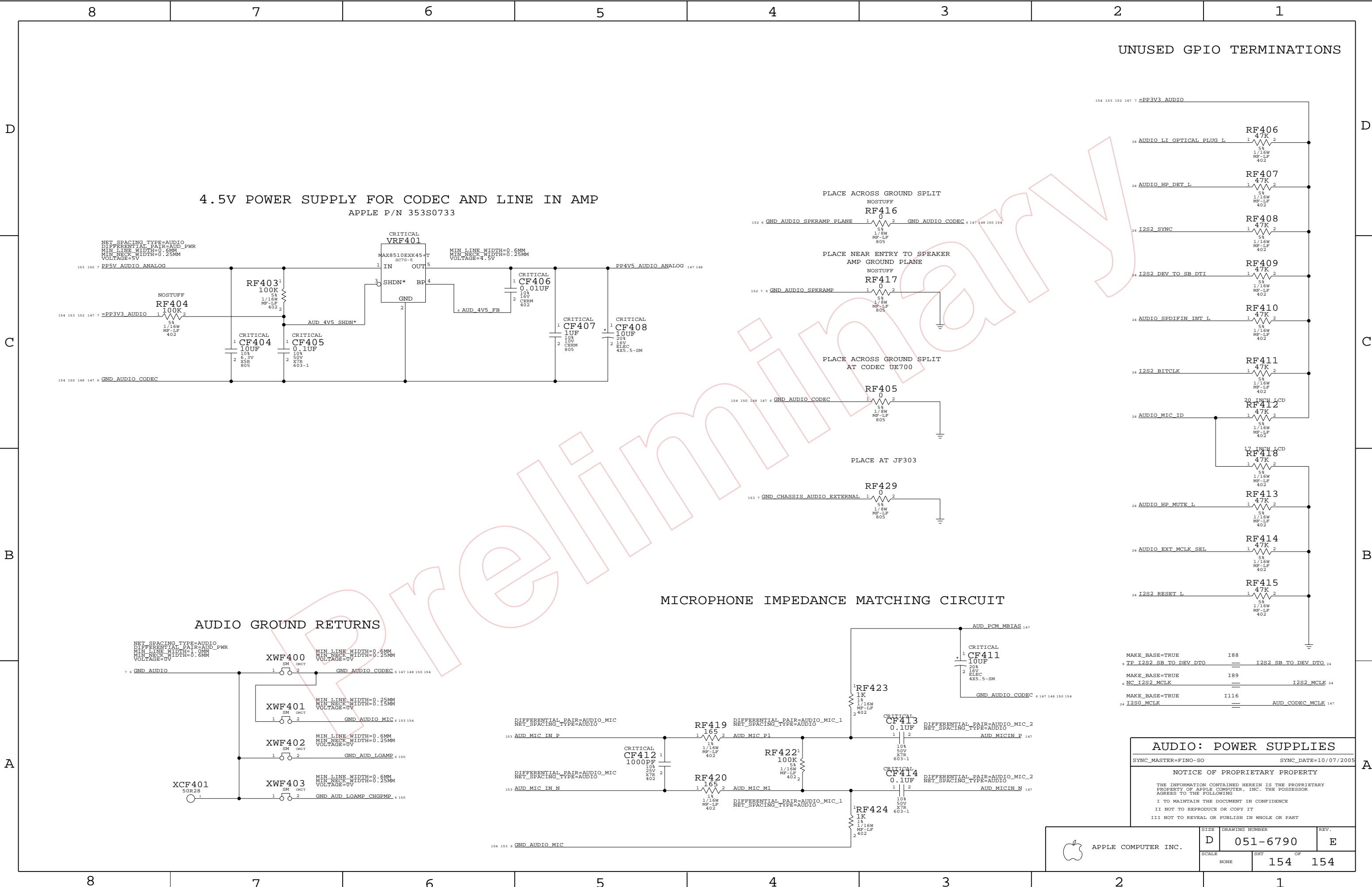
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4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP  
APPLE P/N 353S0733

MICROPHONE IMPEDANCE MATCHING CIRCUIT

AUDIO GROUND RETURNS

UNUSED GPIO TERMINATIONS

AUDIO: POWER SUPPLIES

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